Welcome To

ISSCC 2014
SESSION 15

Digital PLLs

A 0.0066mm^2 780μW Fully Synthesizable PLL with a Current Output DAC and an Interpolative Phase-Coupled Oscillator using Edge Injection Technique

Wei Deng, Dongsheng Yang, Tomohiro Ueno,
Teerachot Siriburanon, Satoshi Kondo,
Kenichi Okada, and Akira Matsuzawa

Tokyo Institute of Technology, Japan

Outline

- Motivation
- Concept of synthesizable analog circuits
- Synthesizable PLL
  - Interpolative phase-coupled oscillator
  - Standard-cell I-DAC
  - Standard-cell varactor
  - Edge injection
- Measurement Results
- Conclusion

Motivation

- **Synthesizable analog circuits**
  - Portability
  - Scalability
  - Layout issues above 20nm
- **Potential applications**
  - PLL
  - ADC, DAC
  - Wireless/Wireline transceivers

Synthesizable Analog Circuits

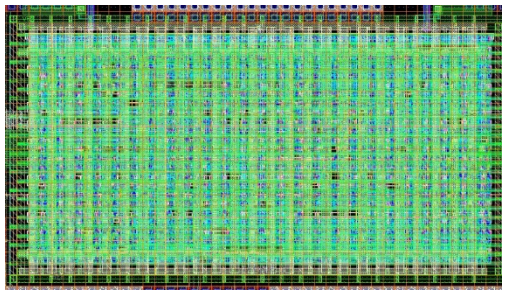
HDL

```
module PLL
(CLK, …, OUT)
…
endmodule
```

Digital design flow

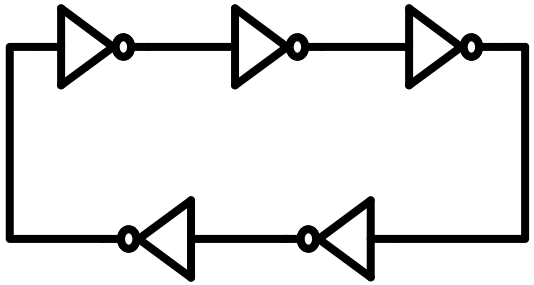
Commercial P&R tools…

GDS

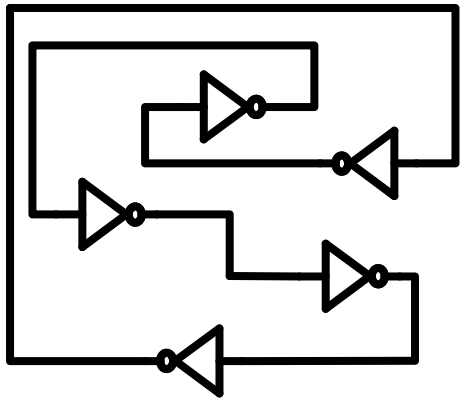


with a standard-cell library
without any custom-designed cells
without manual placement

Issue: Layout Uncertainty



Ideal placement



Actual placement

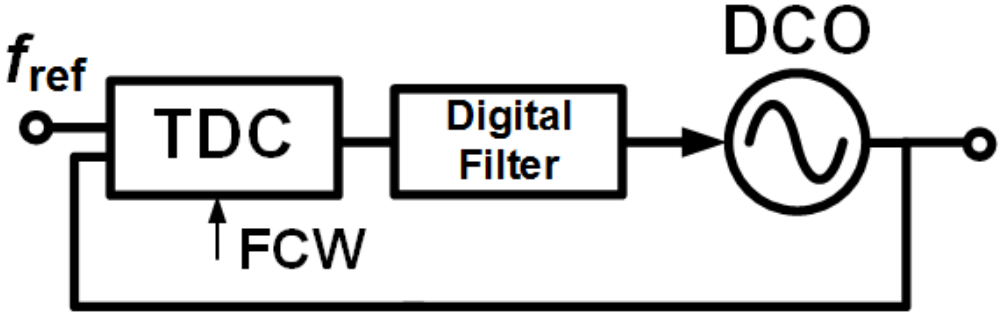
➔Unbalanced loading

No layout symmetry

A new analog-circuit architecture is required, which tolerates layout impairment/uncertainty.

Conventional All-digital PLLs

- TDC-based architecture

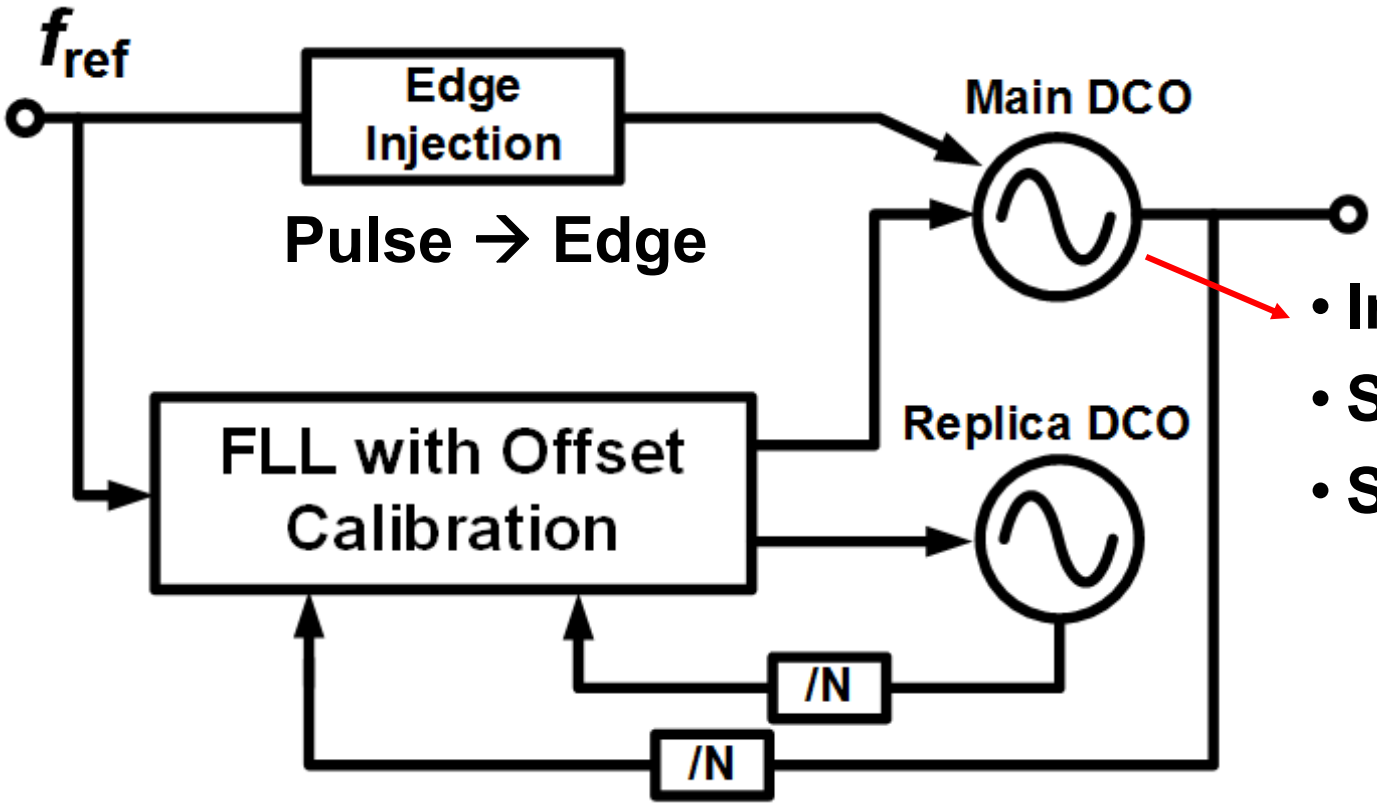


  - The layout uncertainty degrades TDC and DCO linearity.
  - Poor frequency resolution by standard-cell design.
- Trade-off between layout integrity and jitter performance

Proposed Synthesizable PLL

- **Injection-locking topology**
  - Avoid TDC issues (linearity, power-resolution trade-off)
- **Circuit techniques**
  - Interpolative phase-coupled osc. & I-DAC
    - Overcome phase imbalance
  - A new varactor for fine resolution
    - Low spur level
  - Edge injection technique
    - Relax severe timing design

TOP Block Diagram

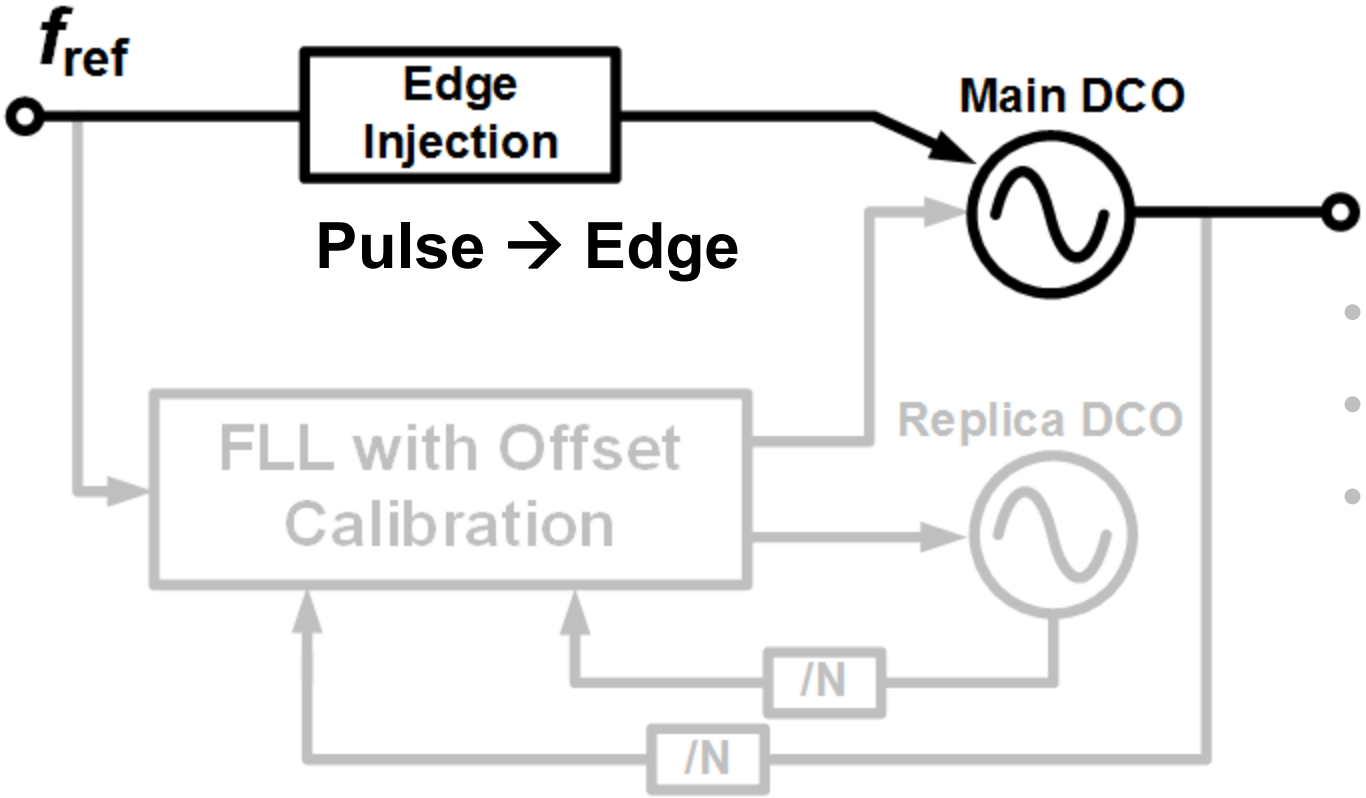


- Interpolation
- Stdcell varactor
- Stdcell I-DAC

[W. Deng, *et al.*, ISSCC 2013]

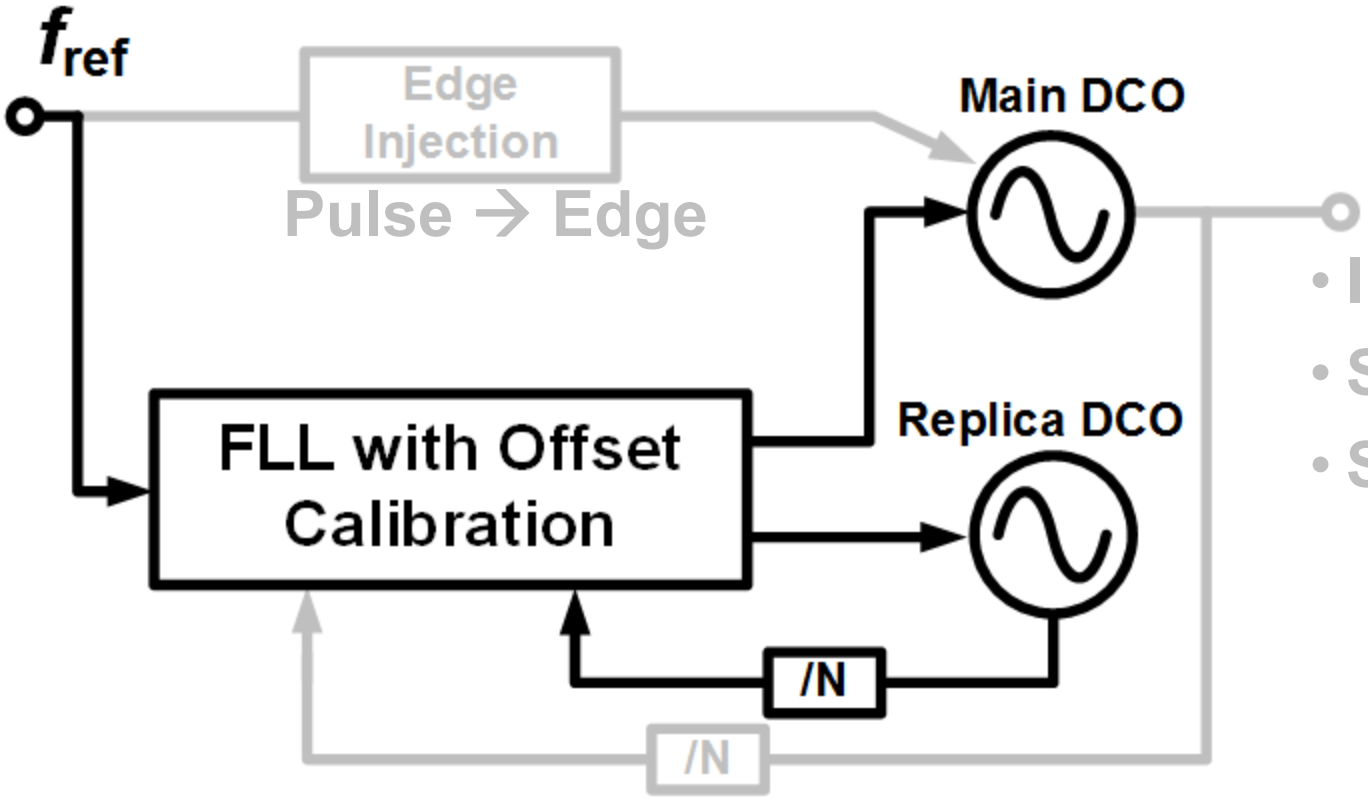
TOP Block Diagram

Feedforward phase locking



- Interpolation
- Stdcell varactor
- Stdcell I-DAC

TOP Block Diagram



- Interpolation
- Stdcell varactor
- Stdcell I-DAC

Feedback FLL for frequency tracking

[W. Deng, *et al.*, ISSCC 2013]

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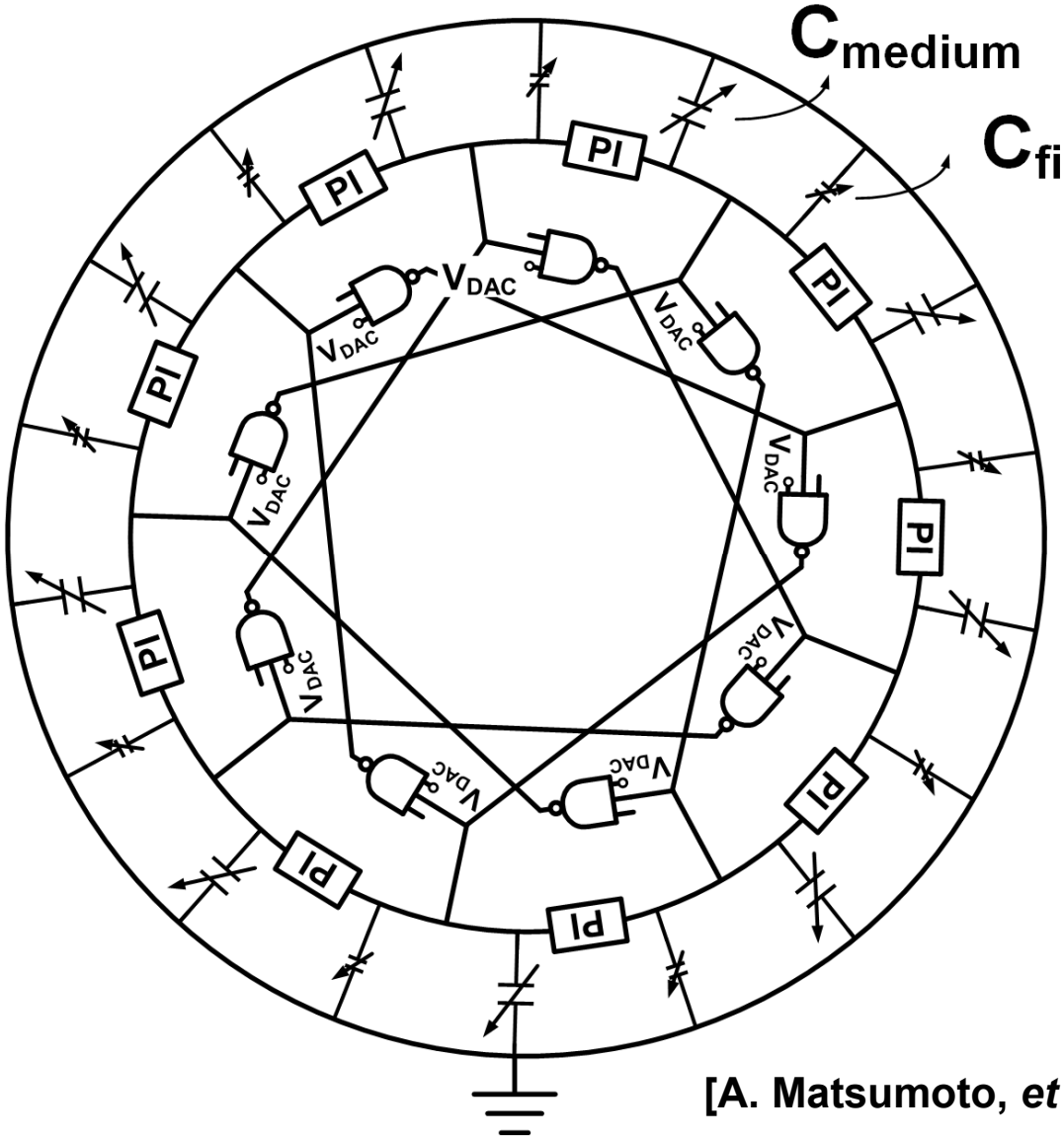
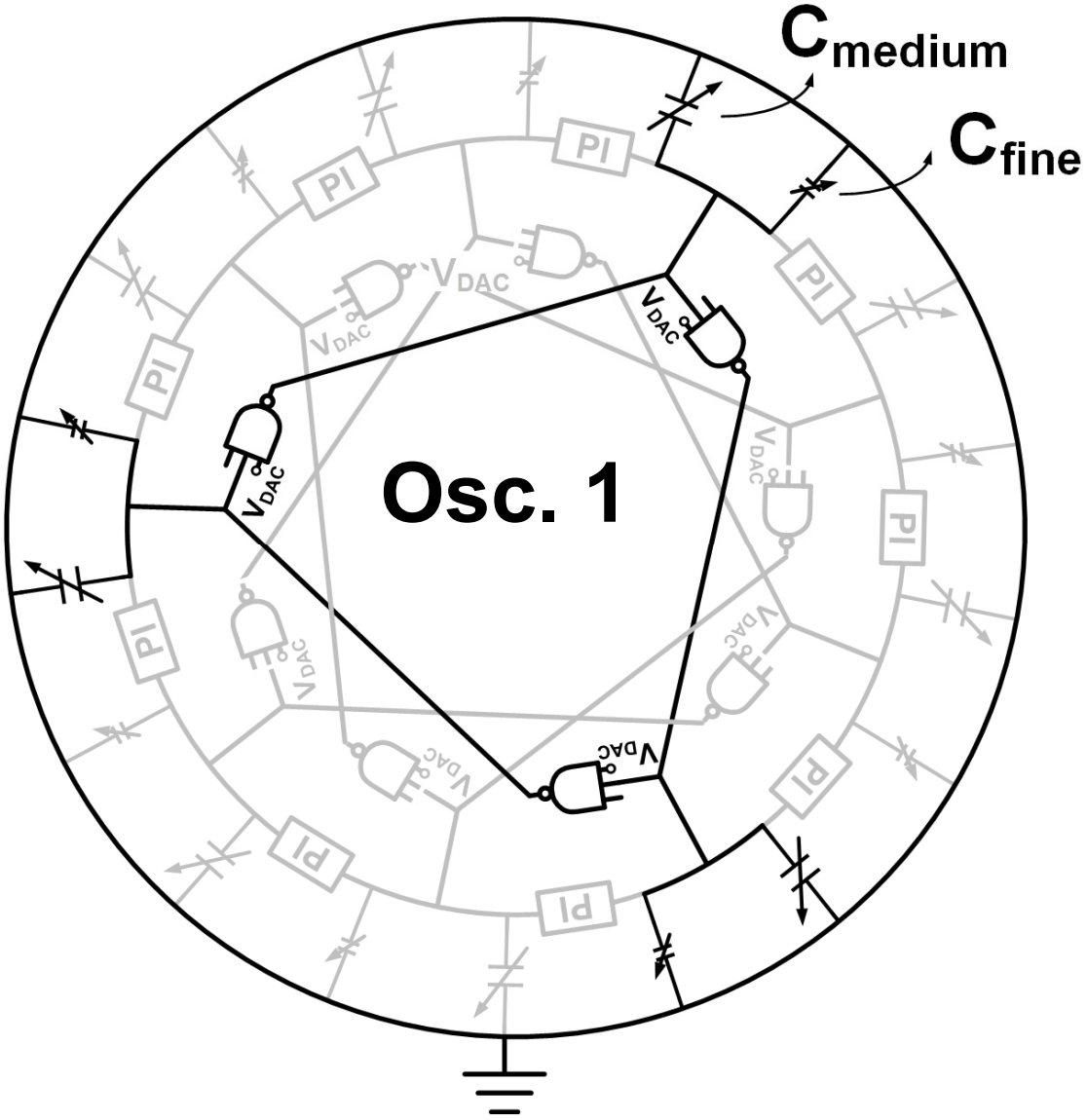
Block Diagram of DCO

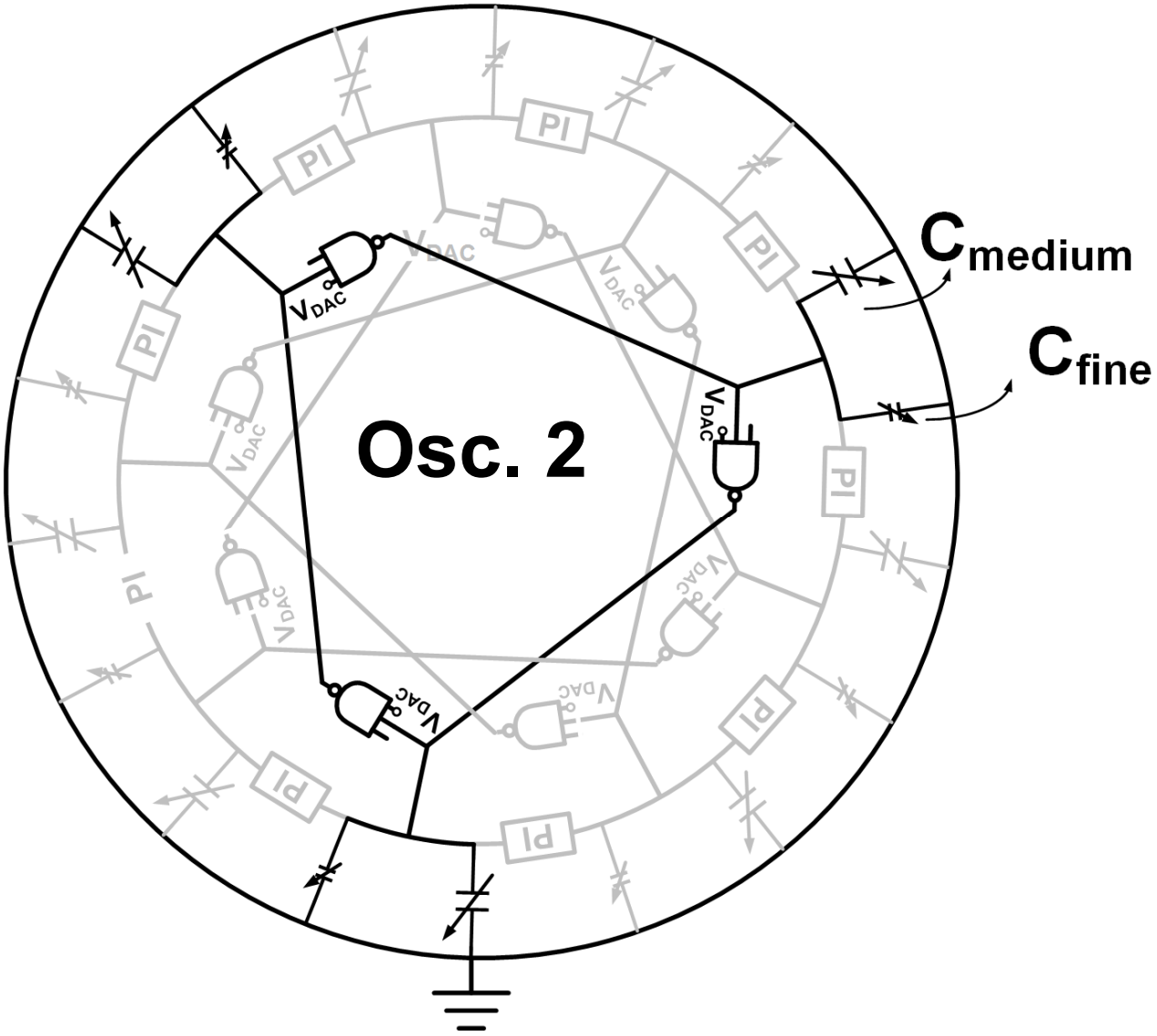


[A. Matsumoto, *et al.*, JSSC 2008]

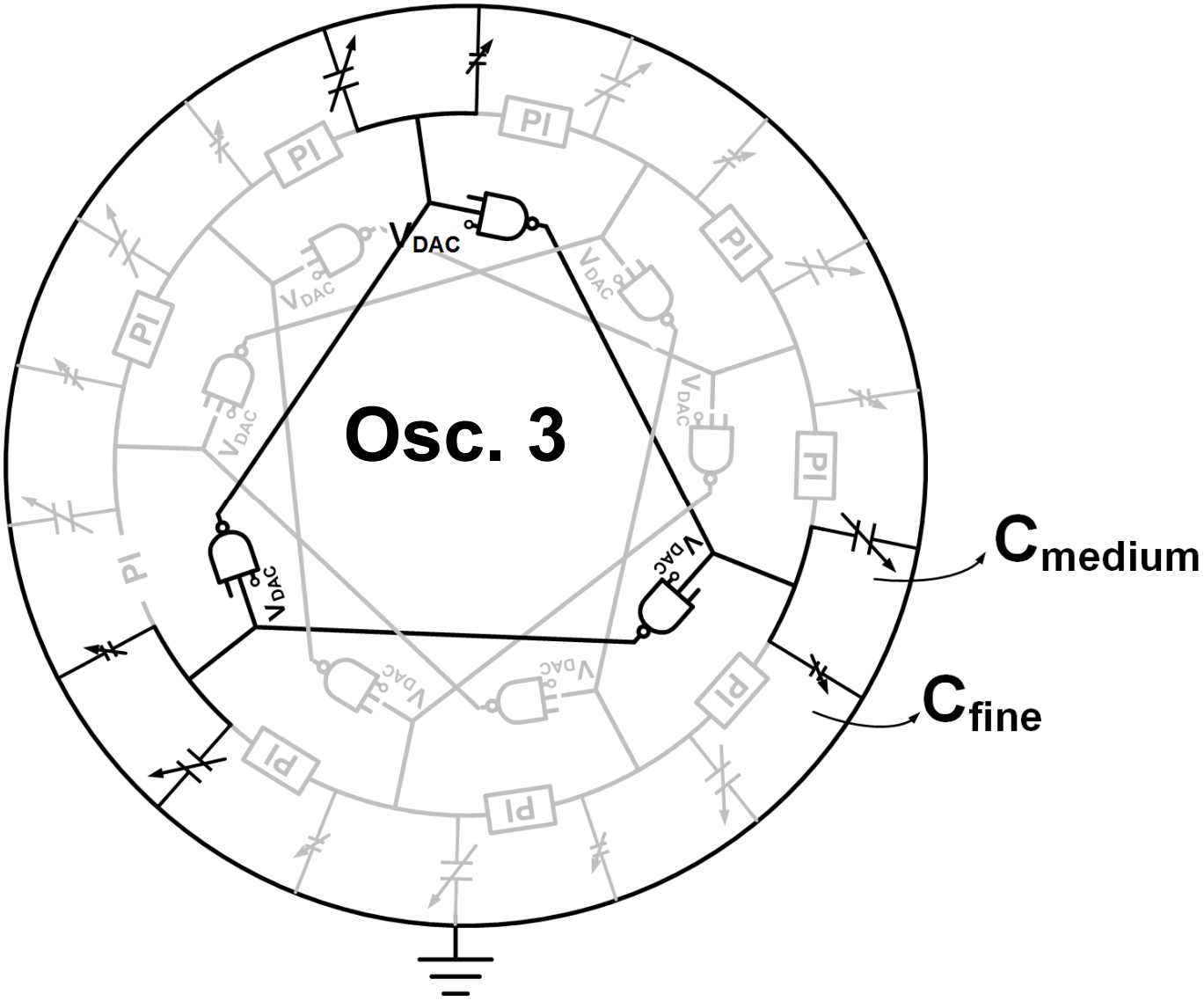
Block Diagram of Oscillator 1



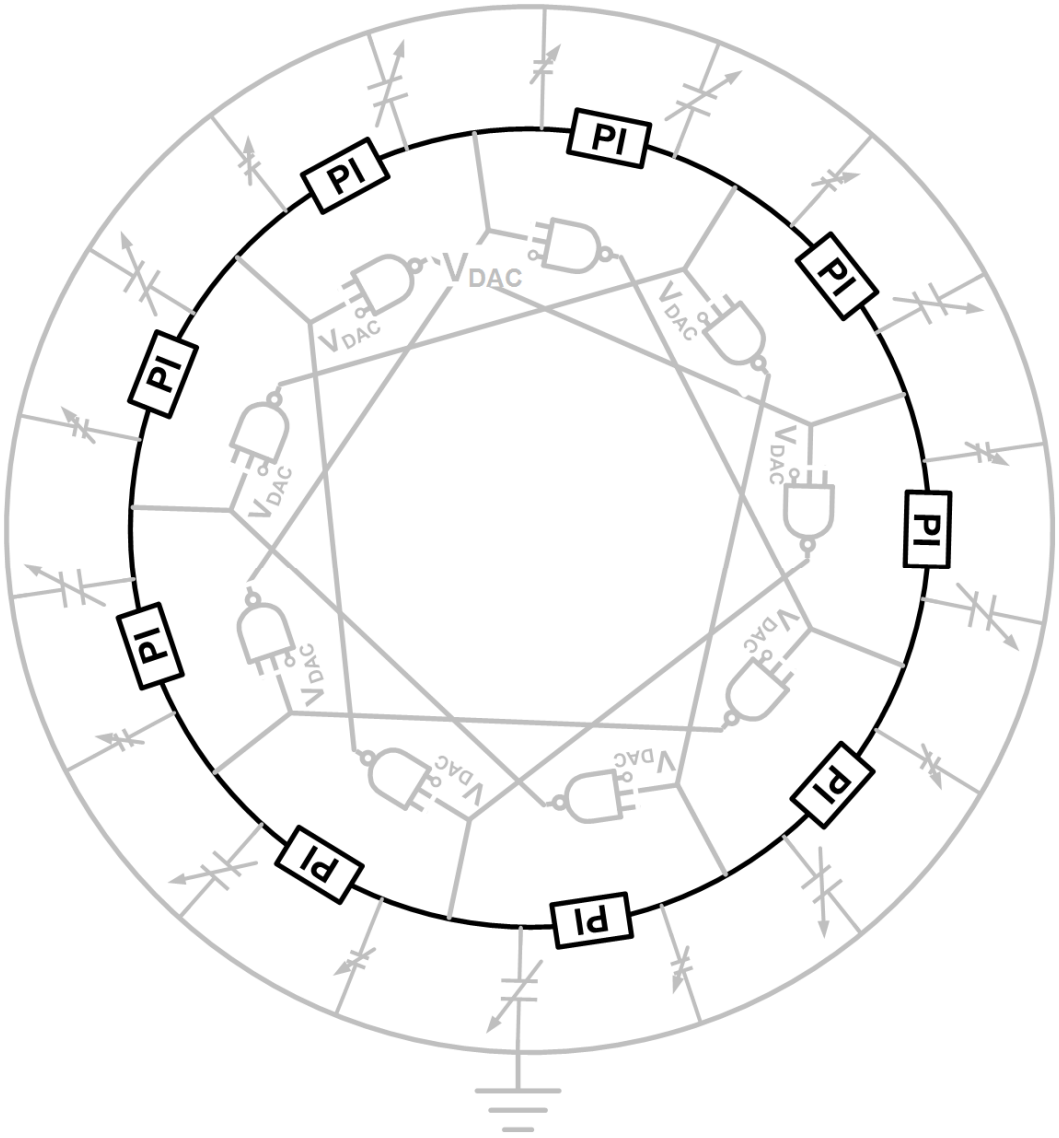
Block Diagram of Oscillator 2



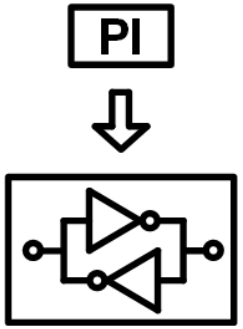
Block Diagram of Oscillator 3



Interpolative Phase-coupled Ring



PI: Phase Interpolator



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  - Edge injection
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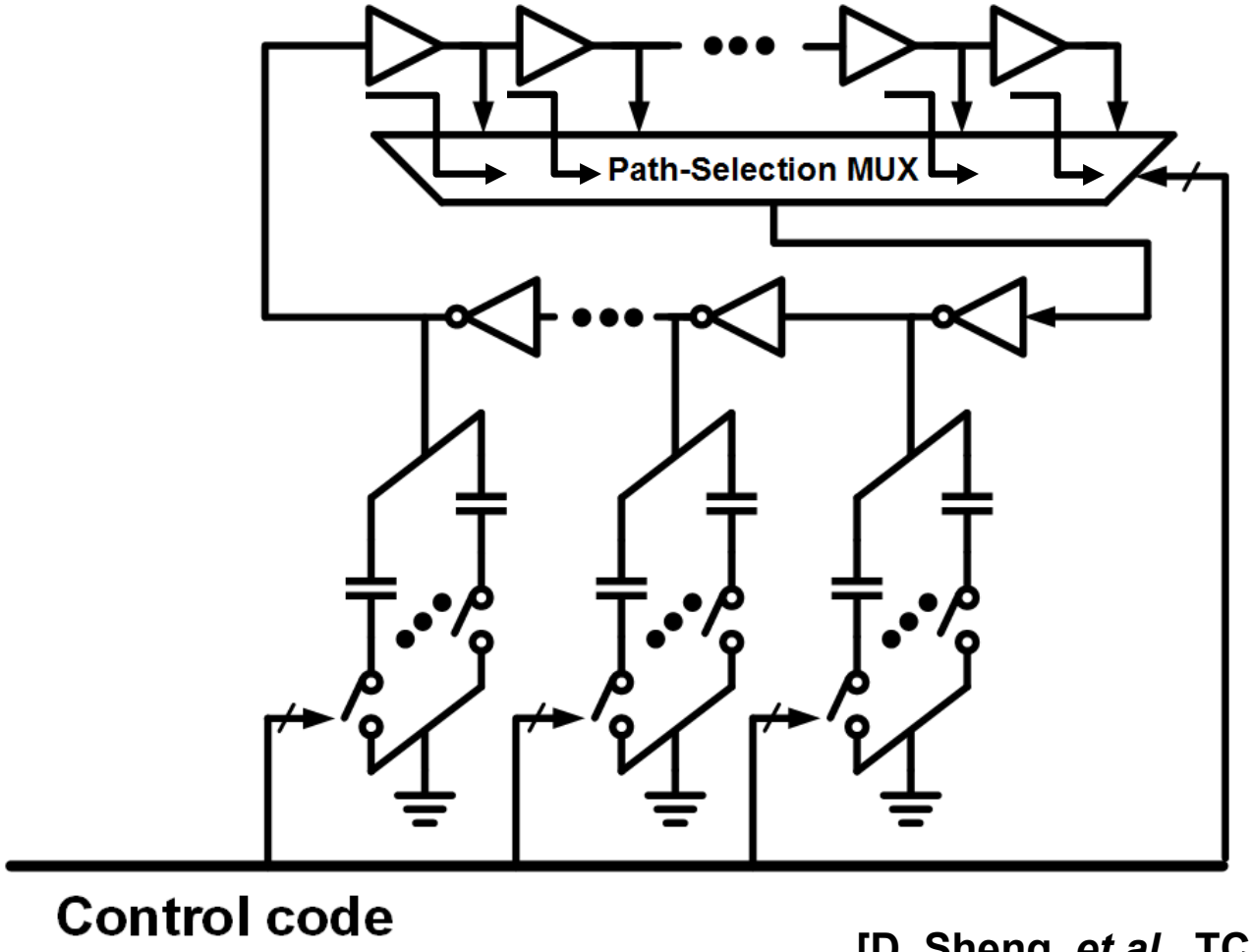
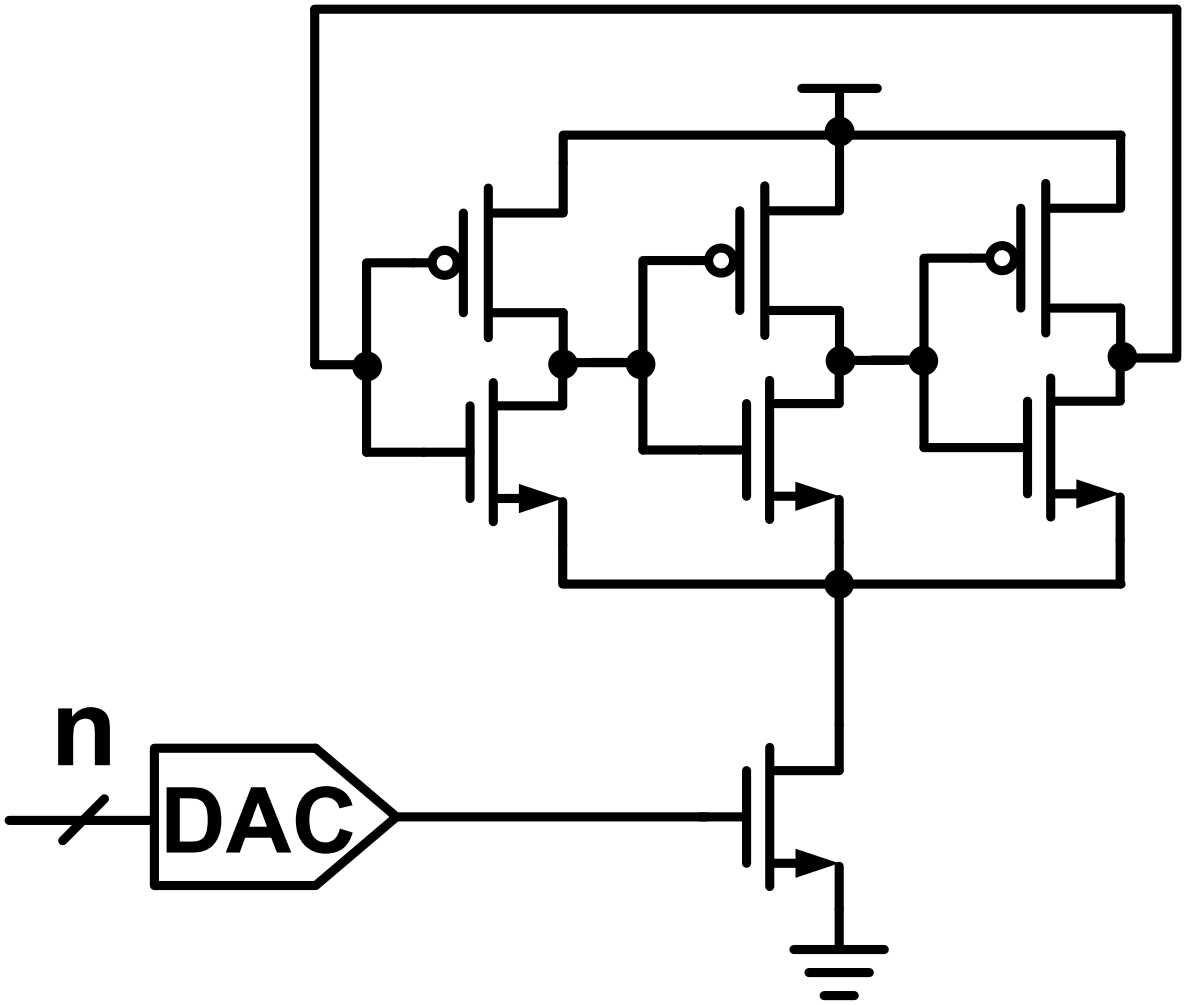
Conventional Coarse Tuning

Unbalanced loading at each stage.

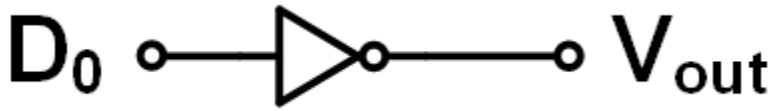


[D. Sheng, *et al.*, TCAS II 2007]

Coarse Tuning using DAC

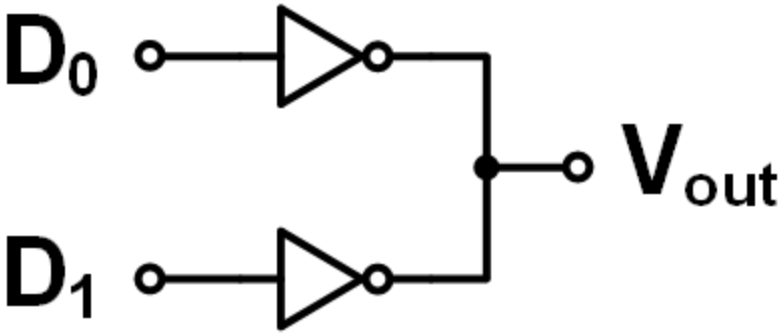


Simple Voltage-output DAC



$D_0 = 0$ $V_{out} = 1V$

$D_0 = 1$ $V_{out} = 0V$



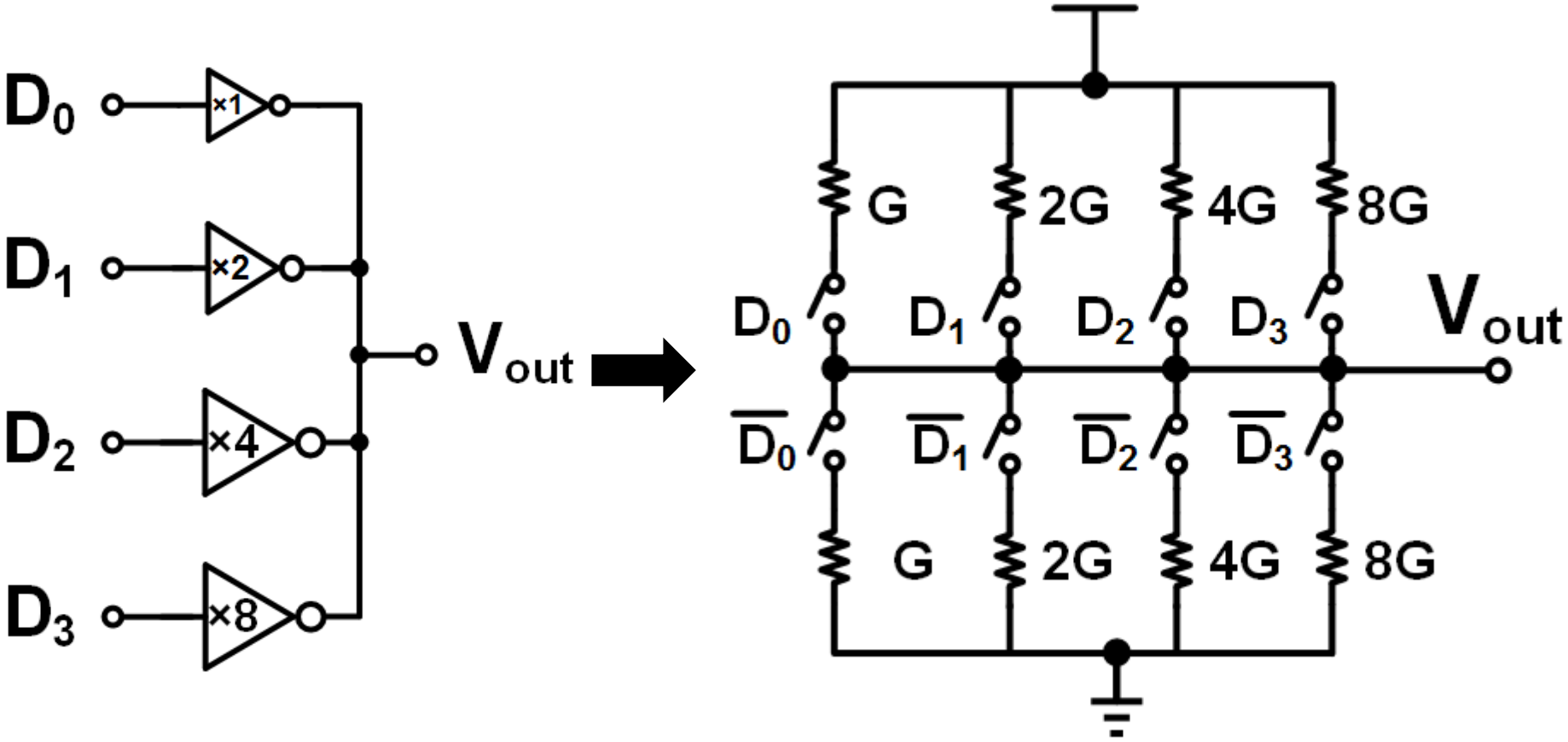
$D_0D_1 = 11$ $V_{out} = 0V$

$D_0D_1 = 10$ $V_{out} = 0.5V$

$D_0D_1 = 01$ $V_{out} = 0.5V$

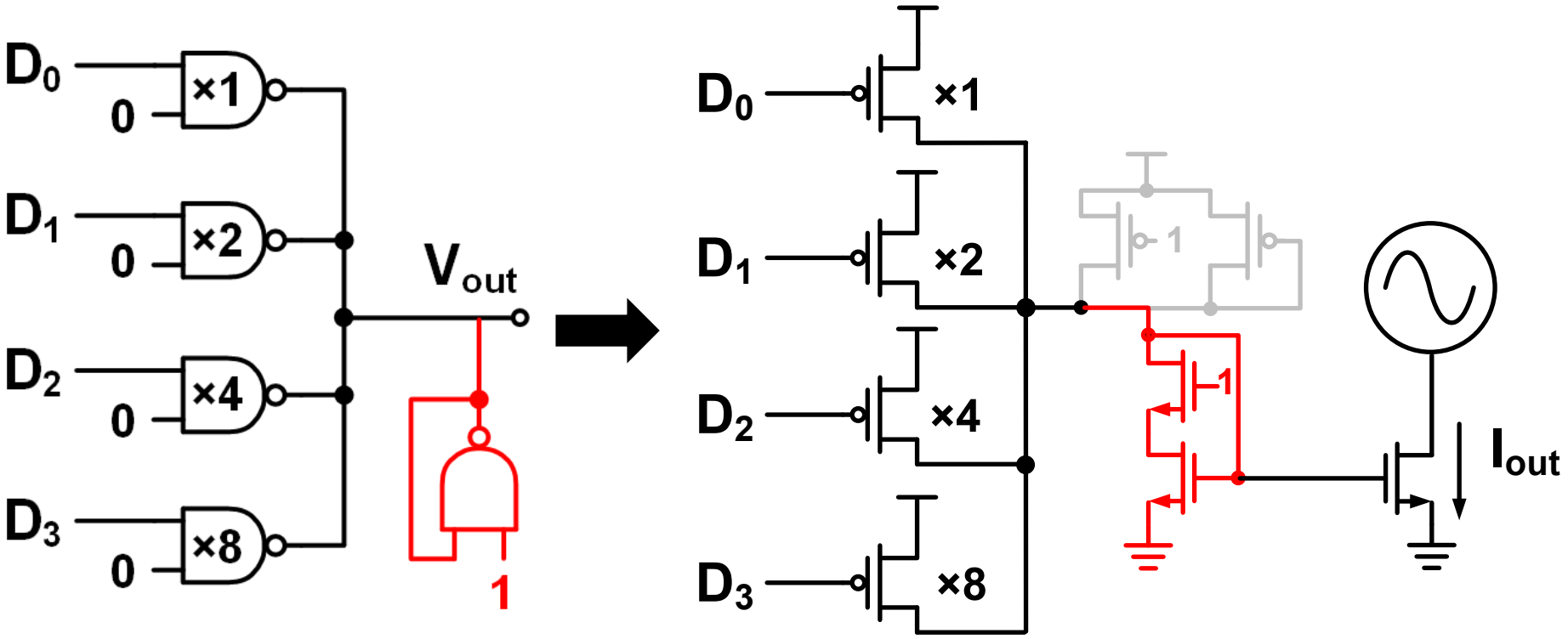
$D_0D_1 = 00$ $V_{out} = 1V$

Model of V-linear DAC



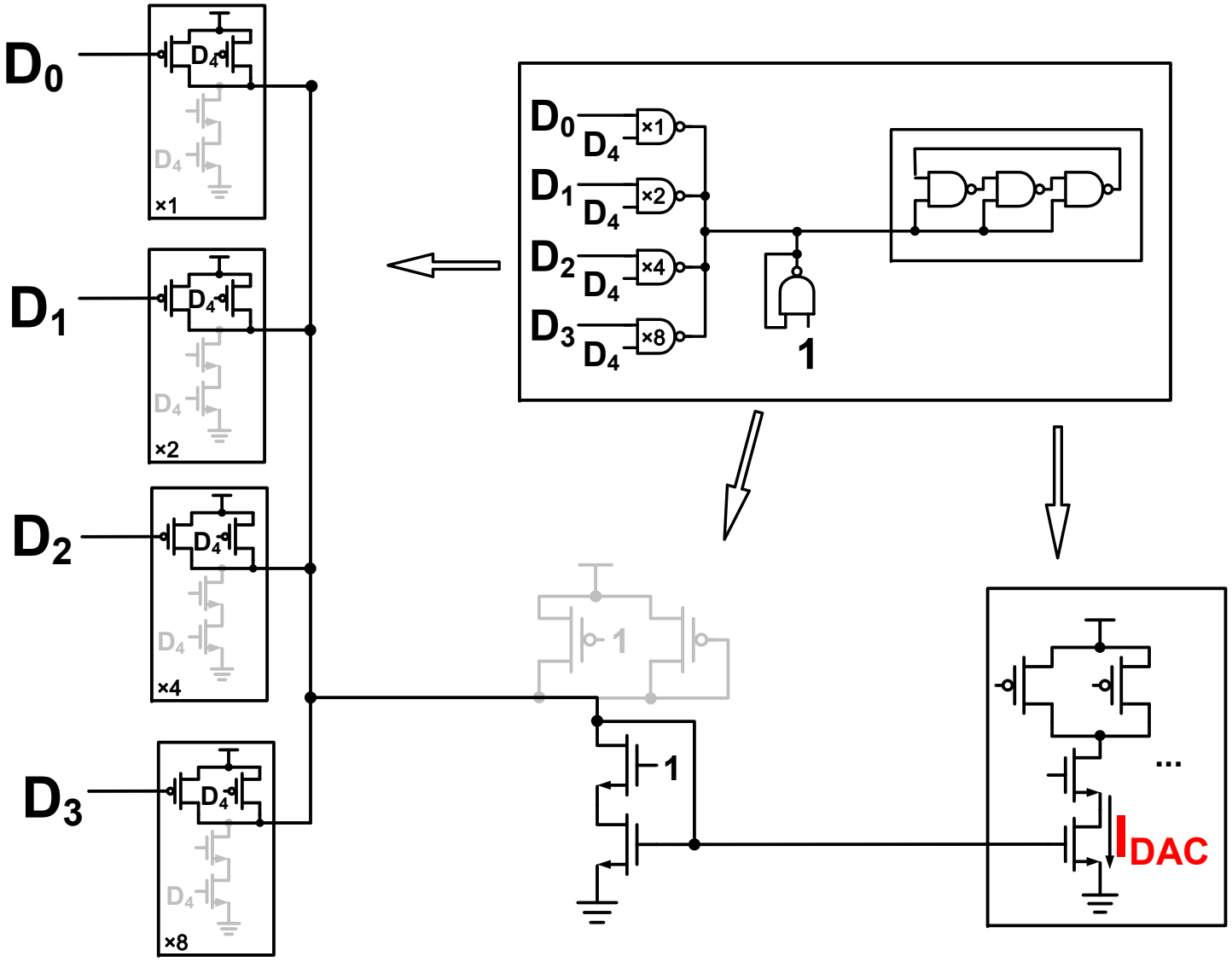
- How to obtain a **I-linear** DAC?

Proposed I-linear DAC

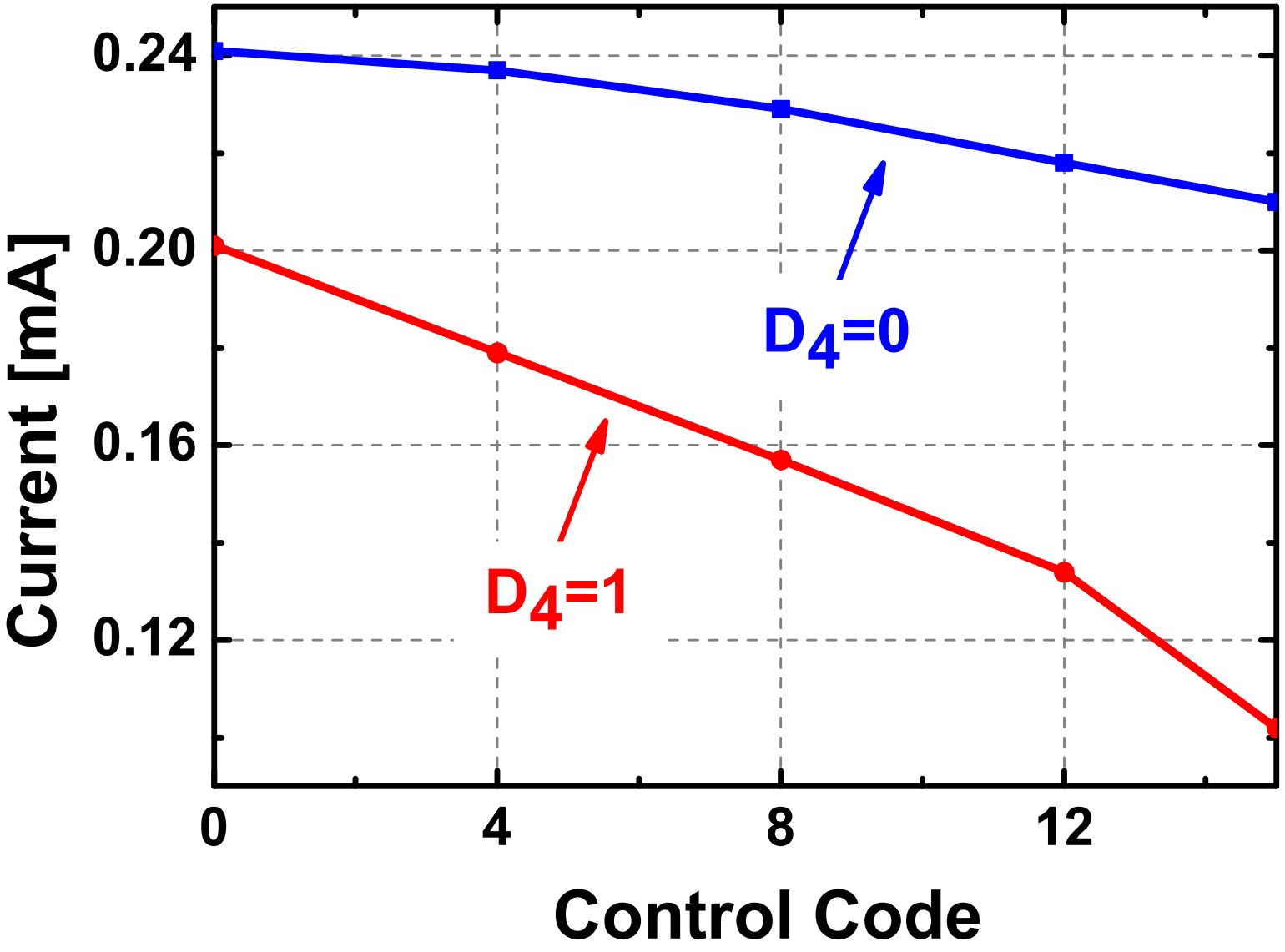


- A feedback structure for forming a current mirror.

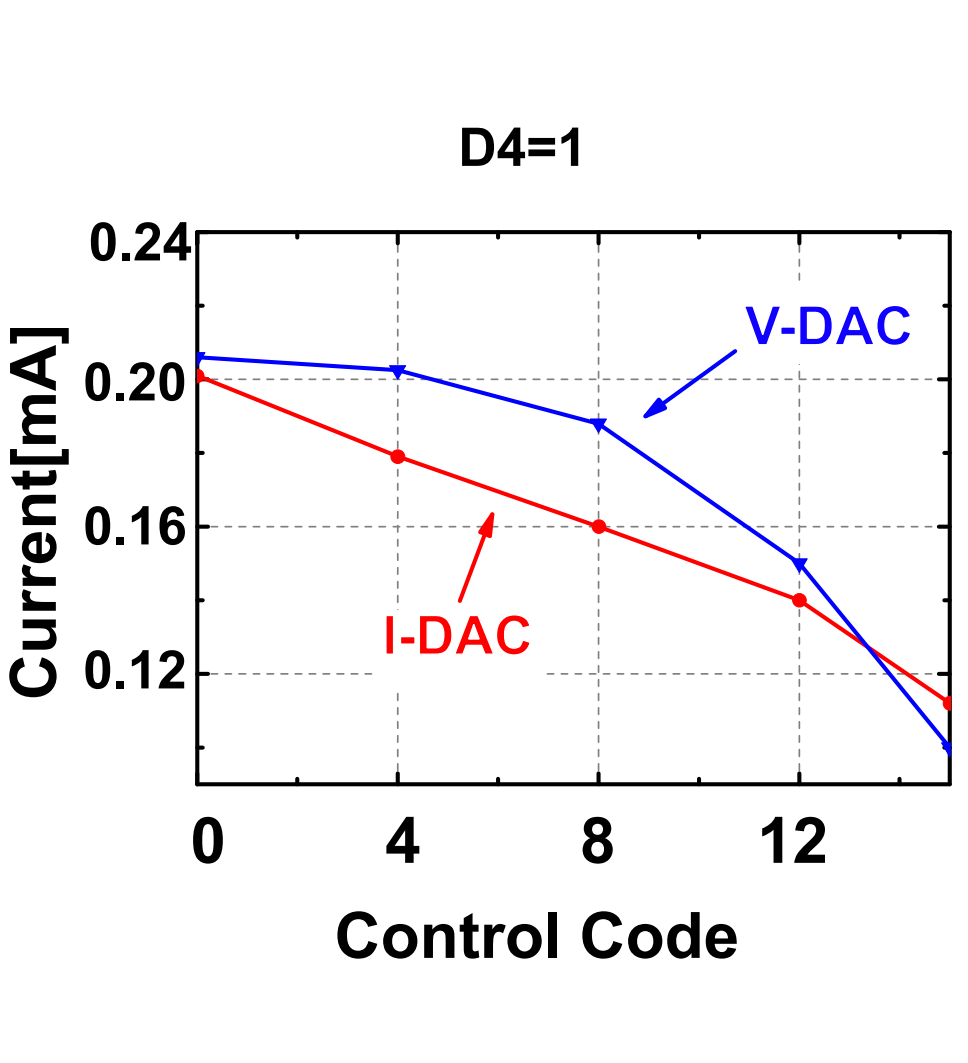
Proposed I-linear DAC (cont.)

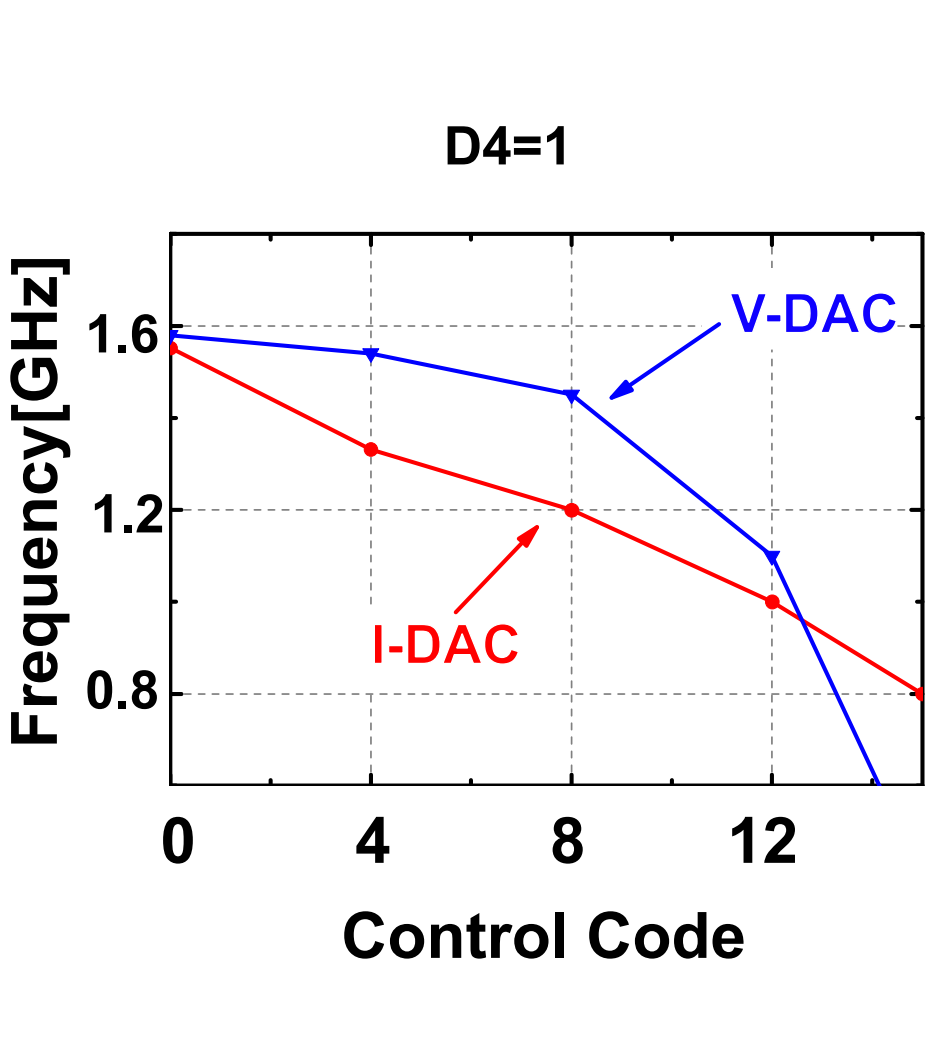


Simulation Result



V-DAC VS I-DAC





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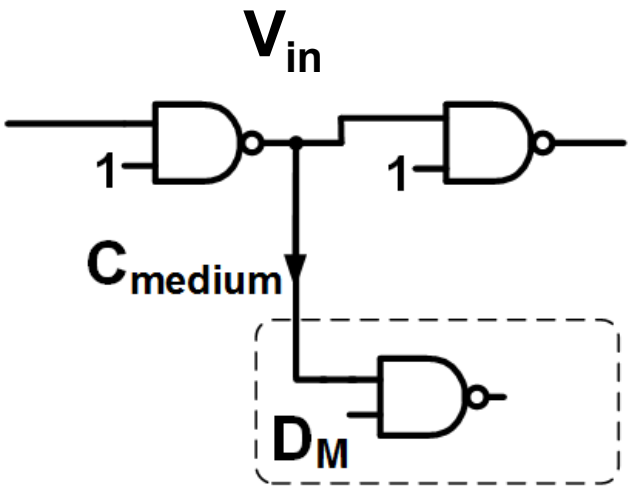
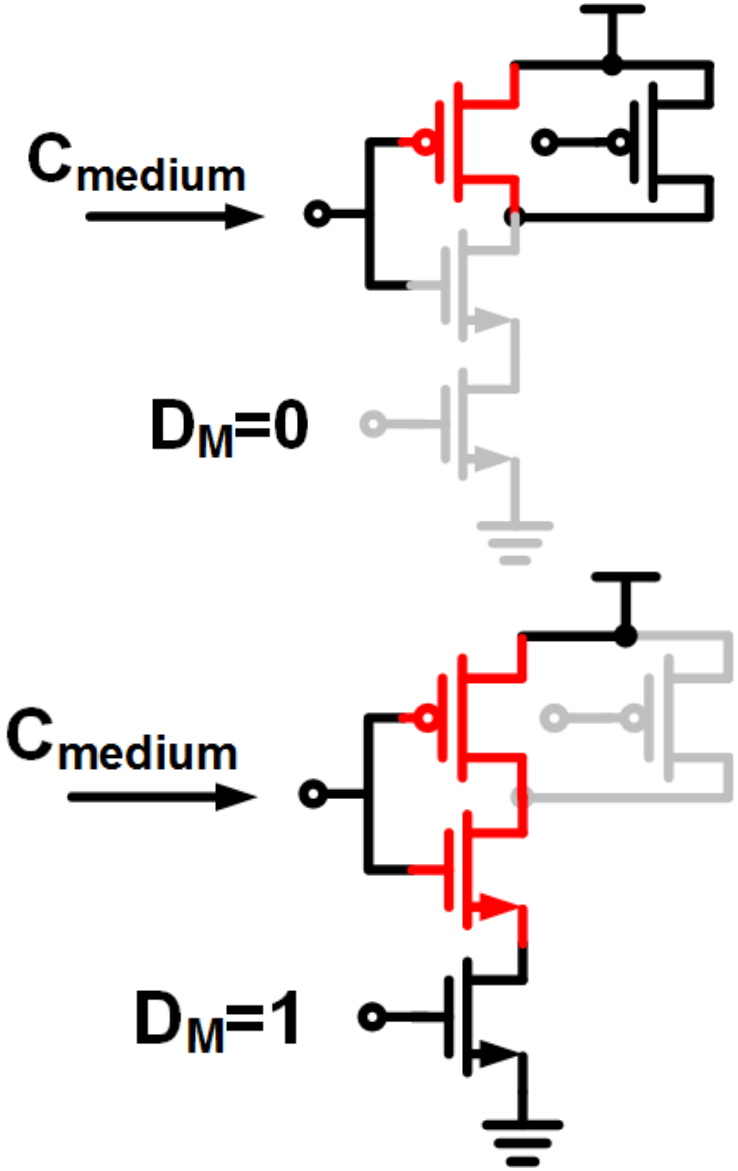
Medium Tuning Capacitor

Conventional:
1.55ps@200MHz

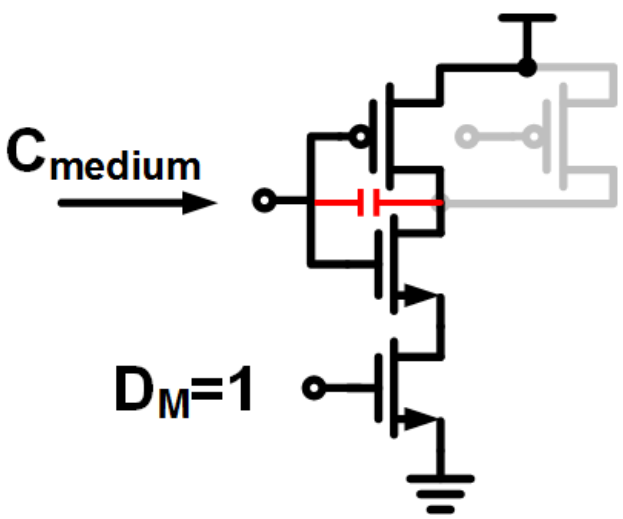


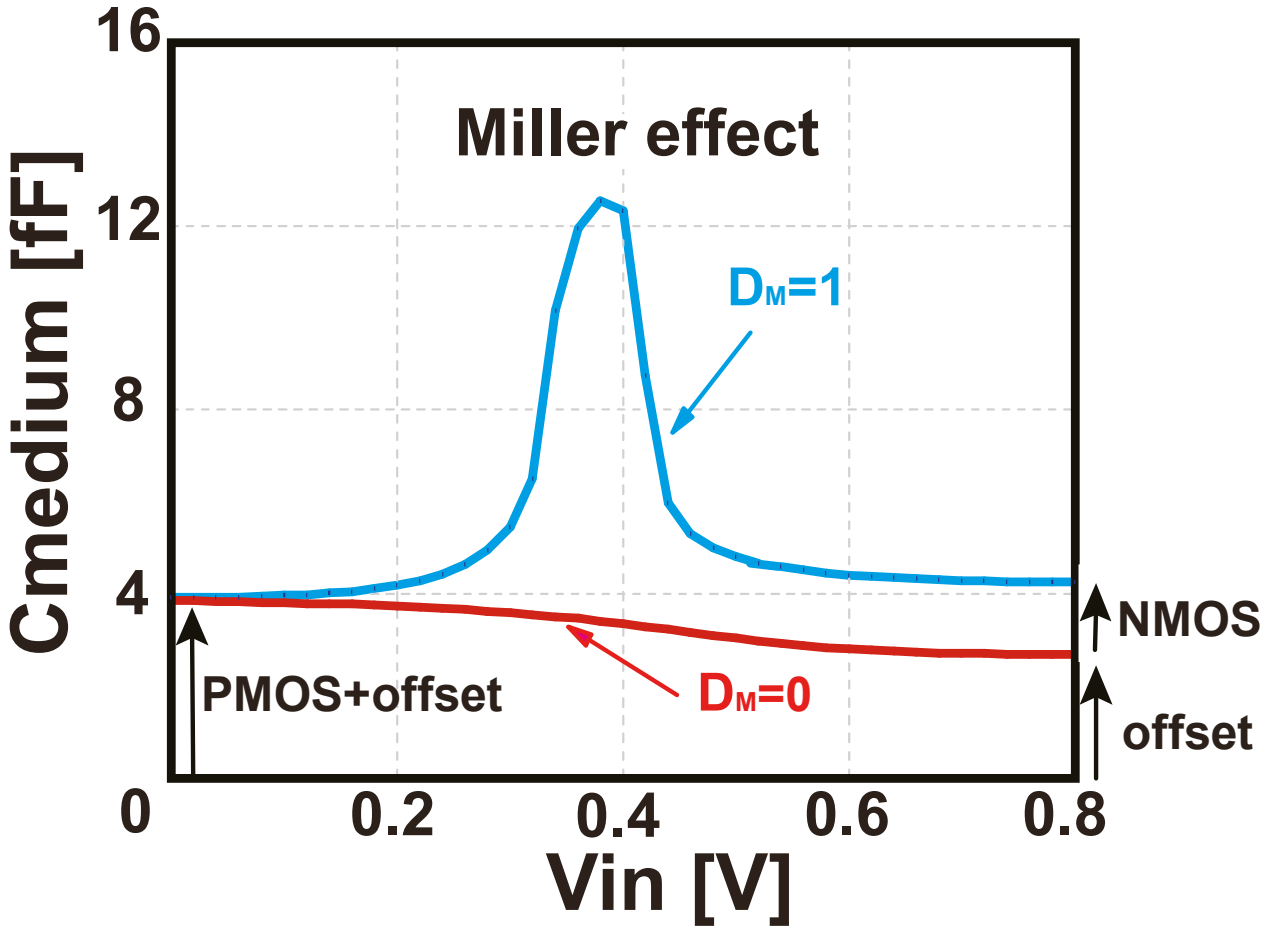
Medium resolution



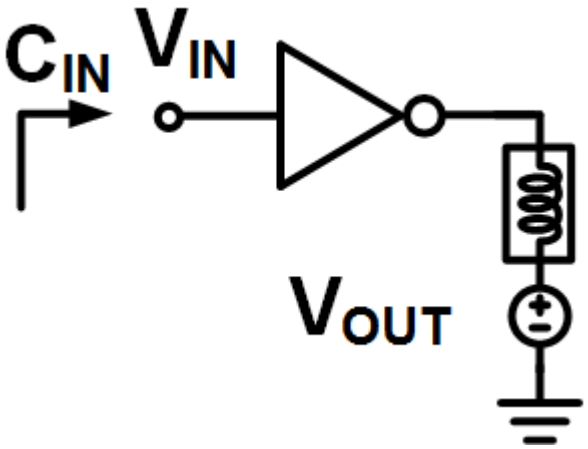
[P.L. Chen, *et al.,* TCAS II 2005]

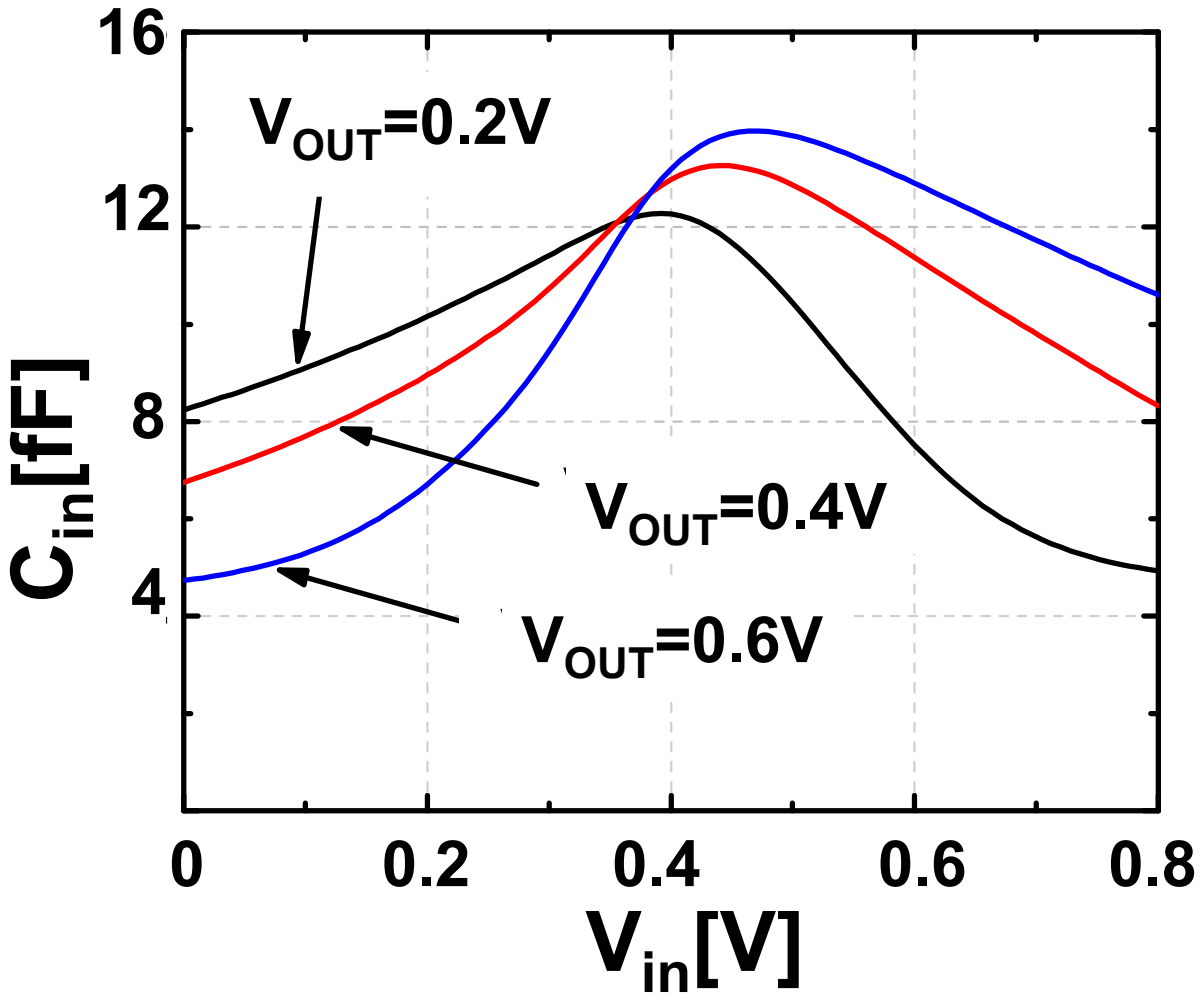
Simulated C_{medium} against V_{in}





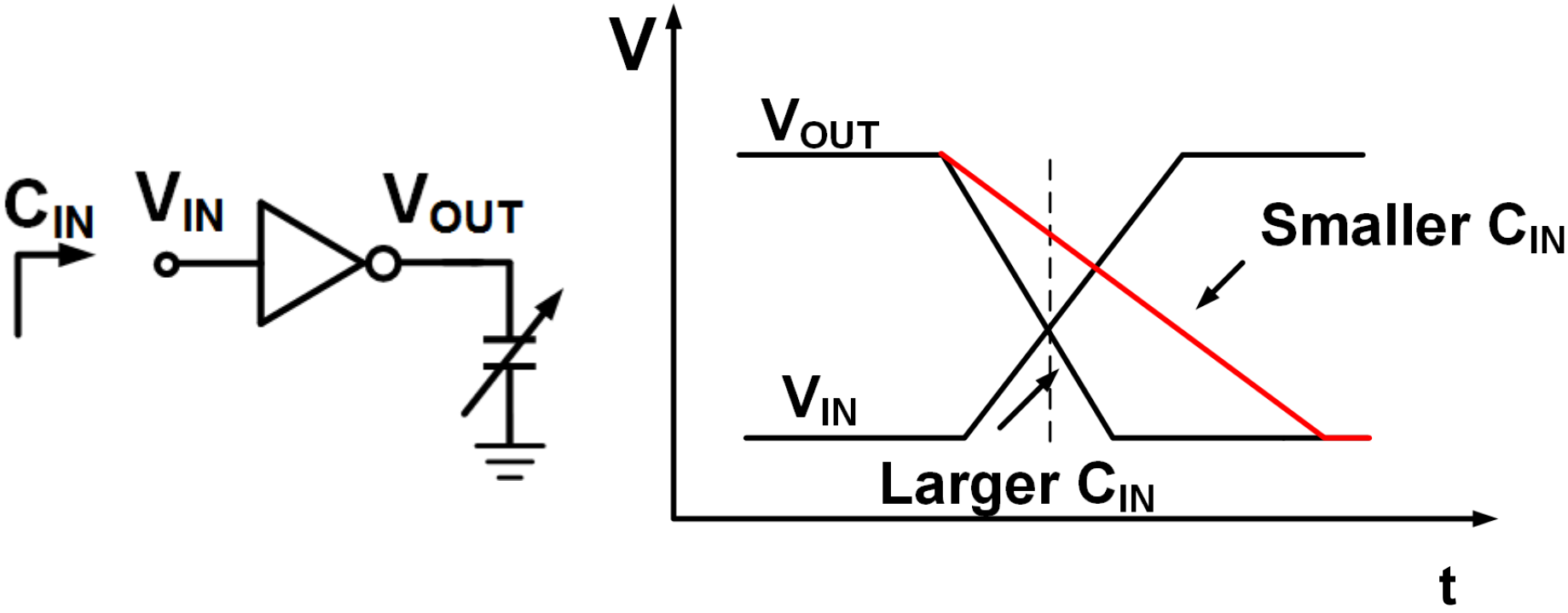
Miller Effect Sensitivity





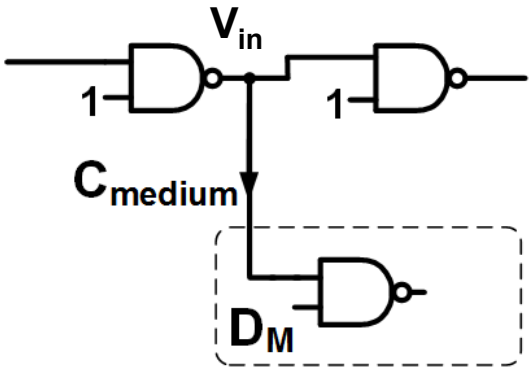
- **Miller effect can be controlled by Vout.**

Miller Effect Sensitivity (Cont.)

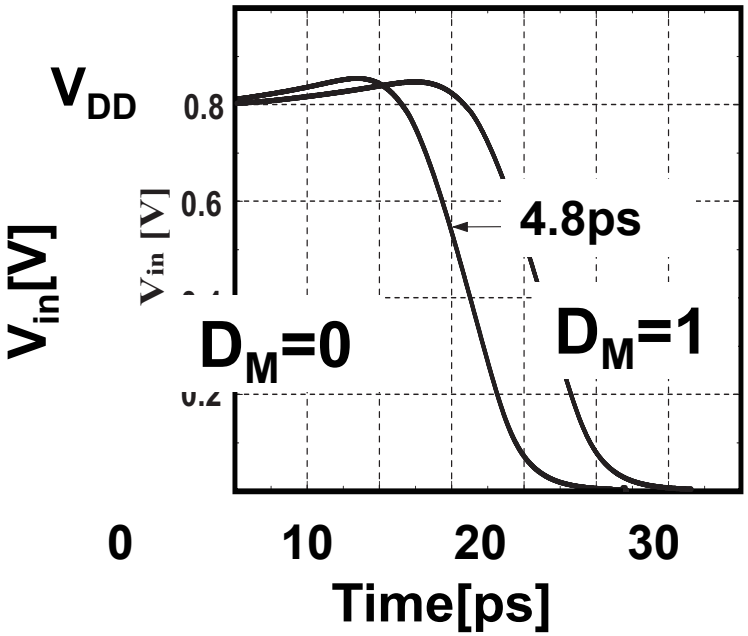


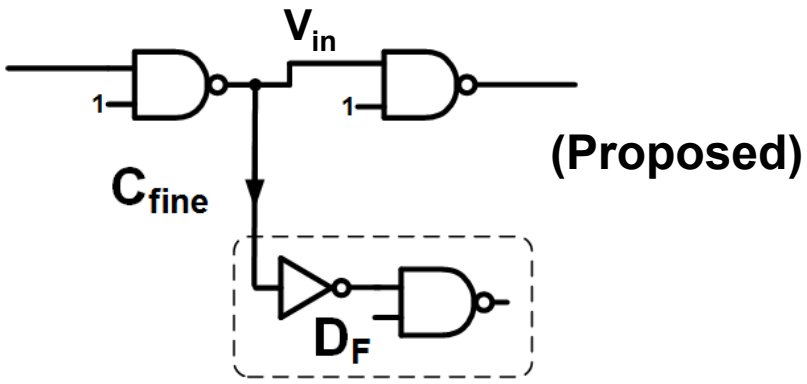
- **A transient variation of V_{OUT} can make a fine capacitance difference in C_{IN}.**

Tuning Capacitors



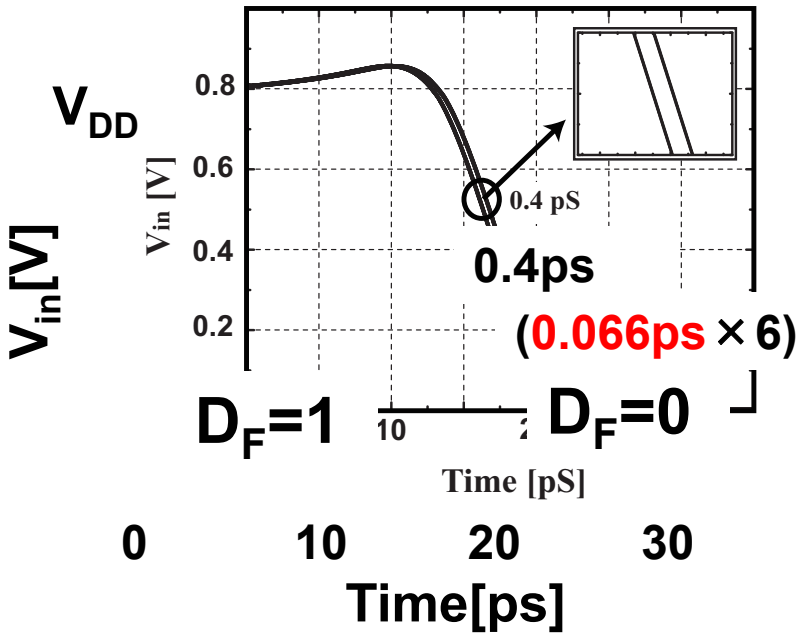
Medium resolution





(Proposed)

Fine resolution



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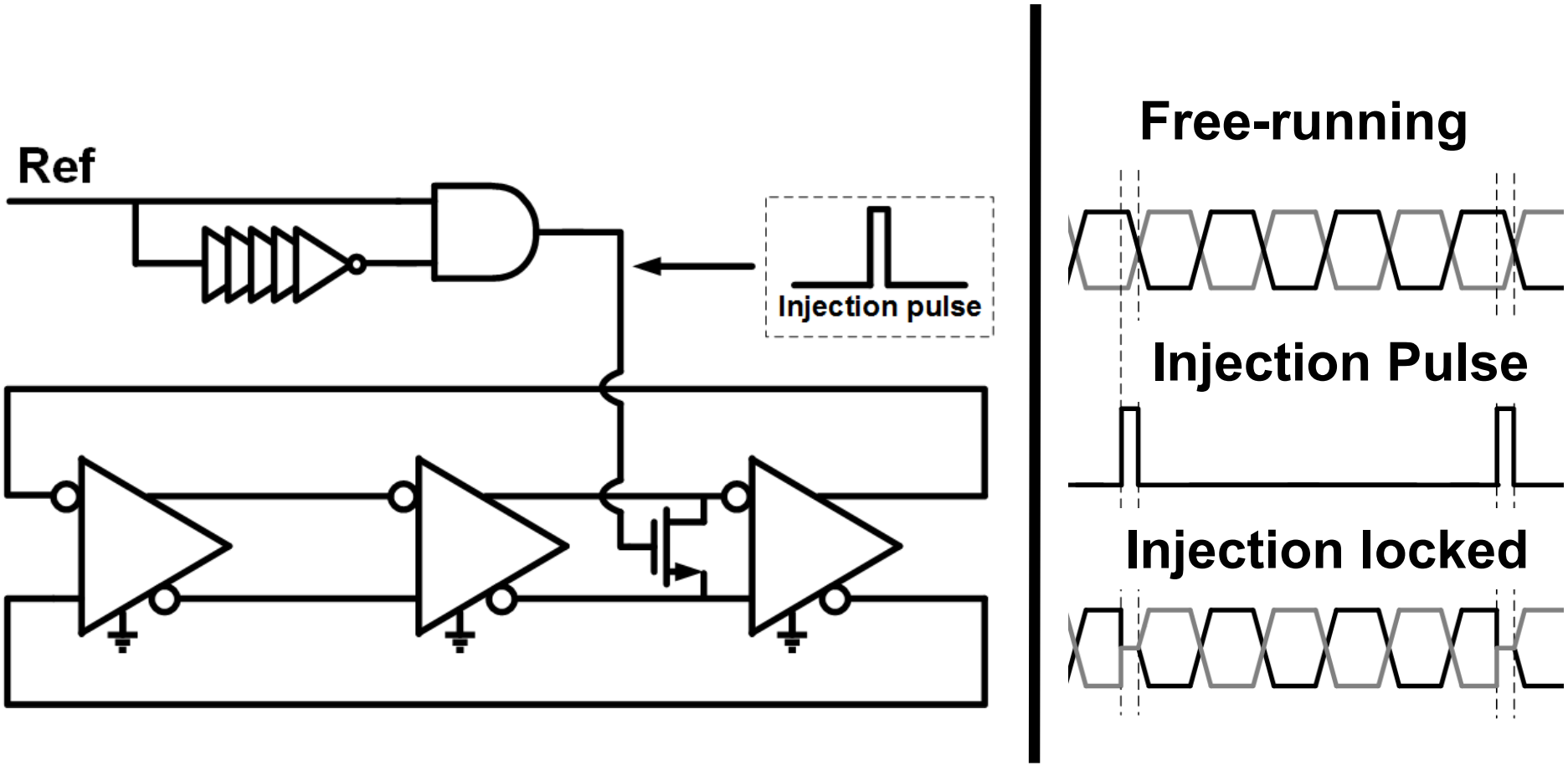
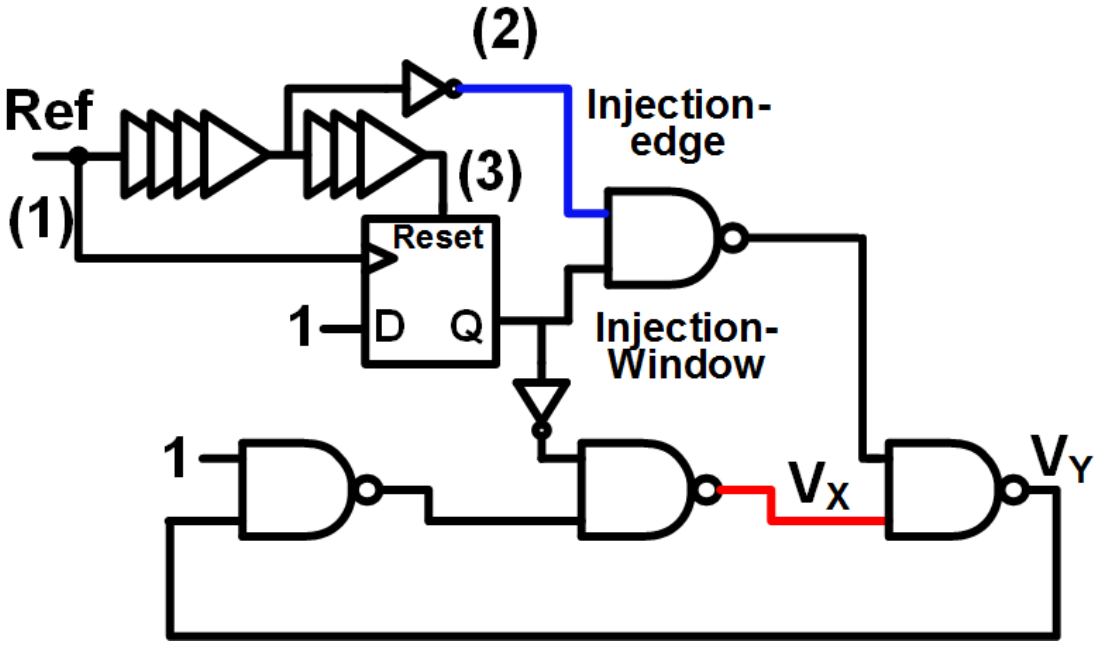
Conventional Pulse Injection

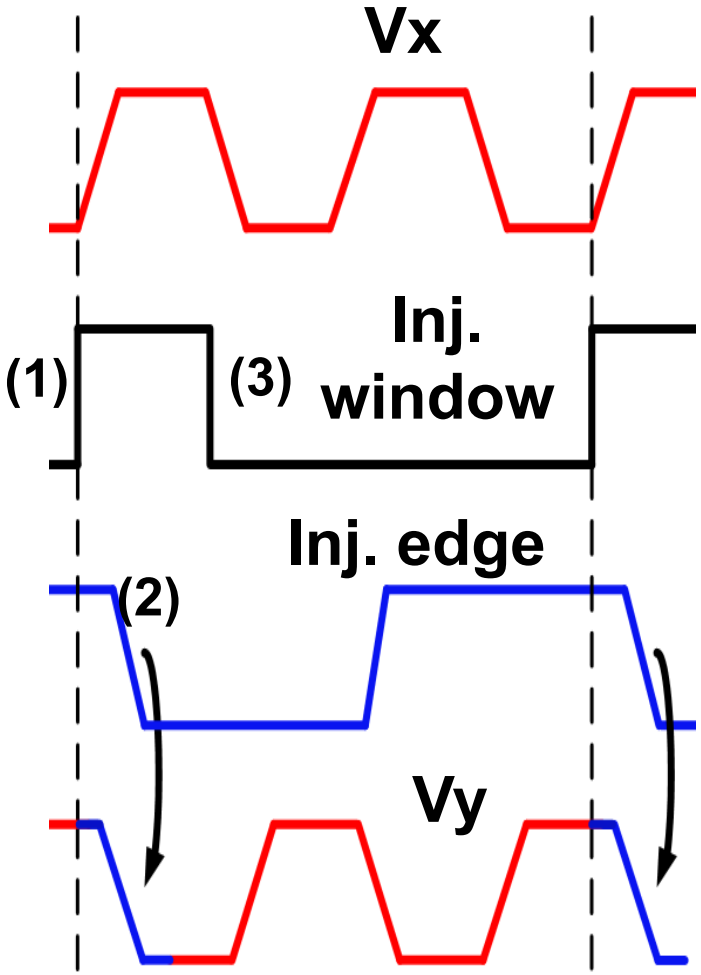


- **Severe timing design** is required on the injection pulse width.

[B. Helal, *et al.*, JSSC 2009]

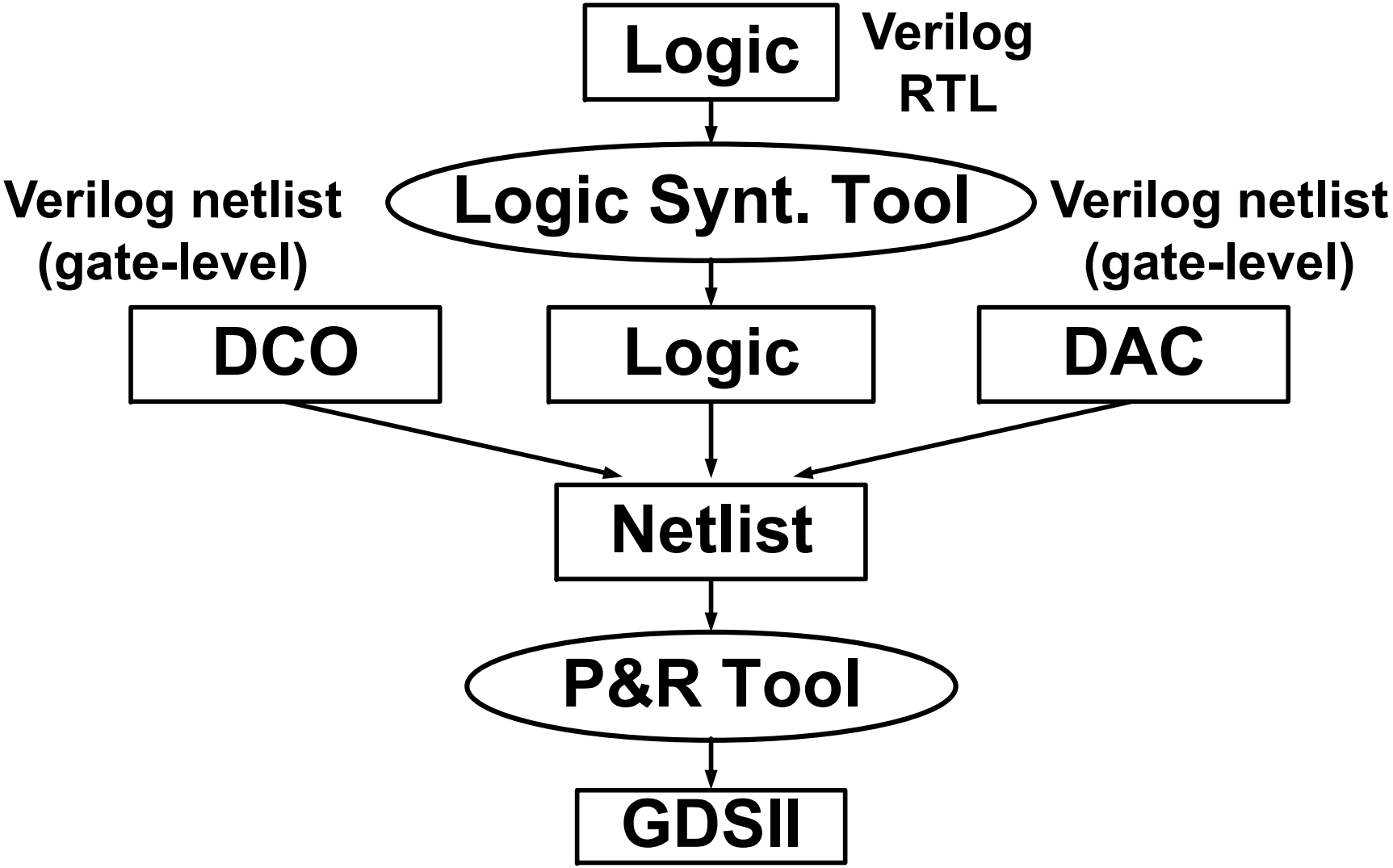
Edge Injection



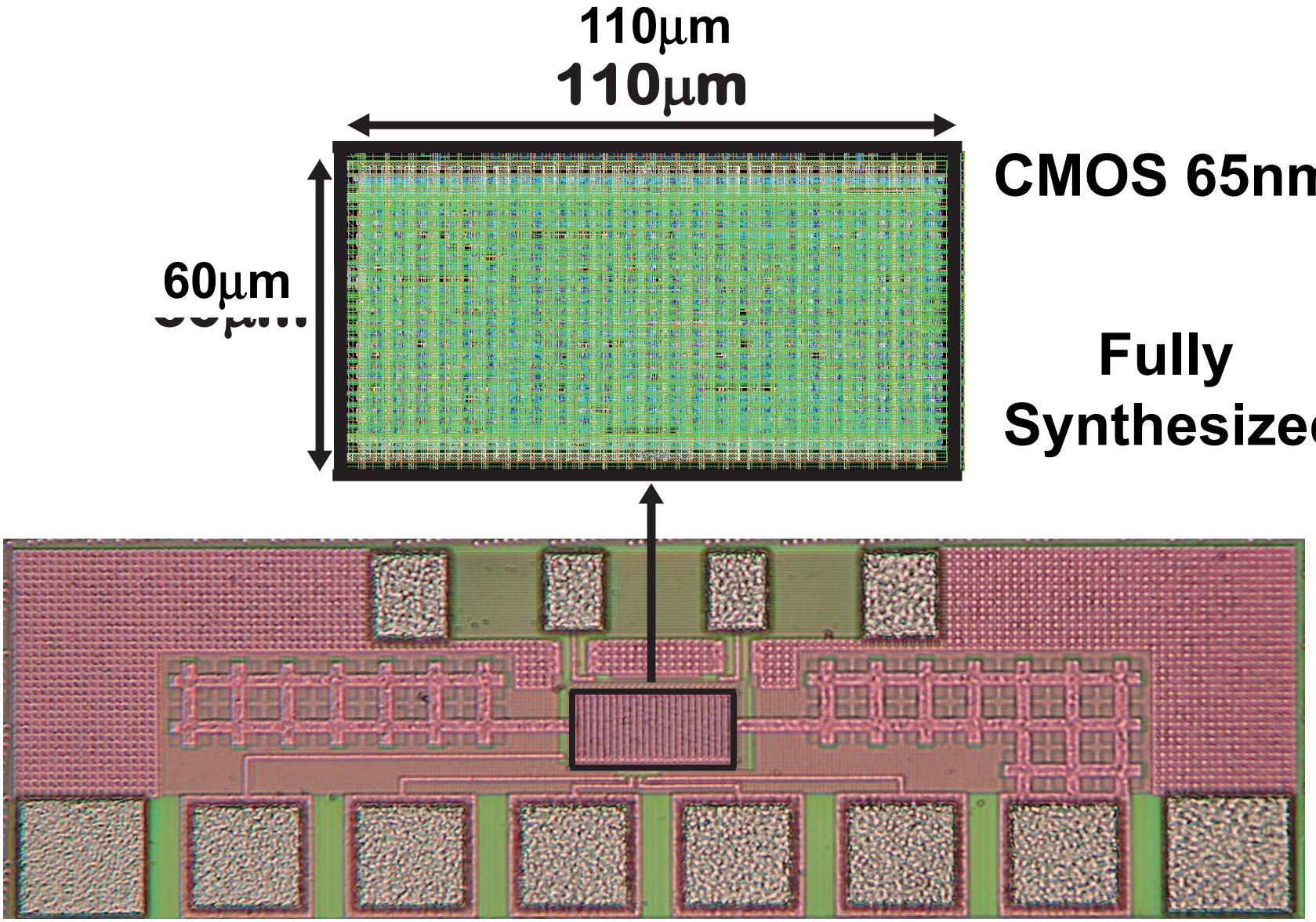


- **Severe timing design is not required.**

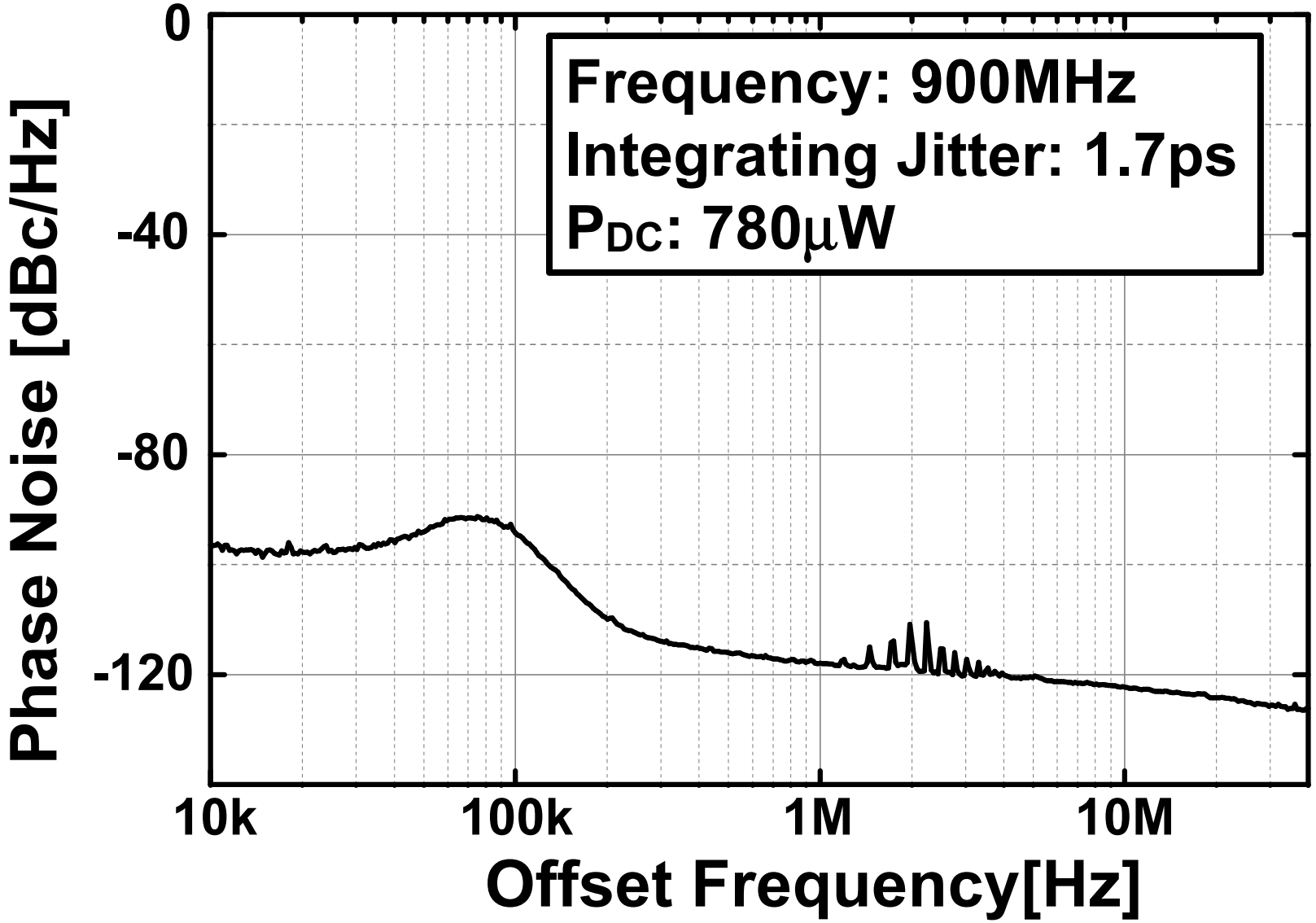
Design Procedure



Chip Microphotograph

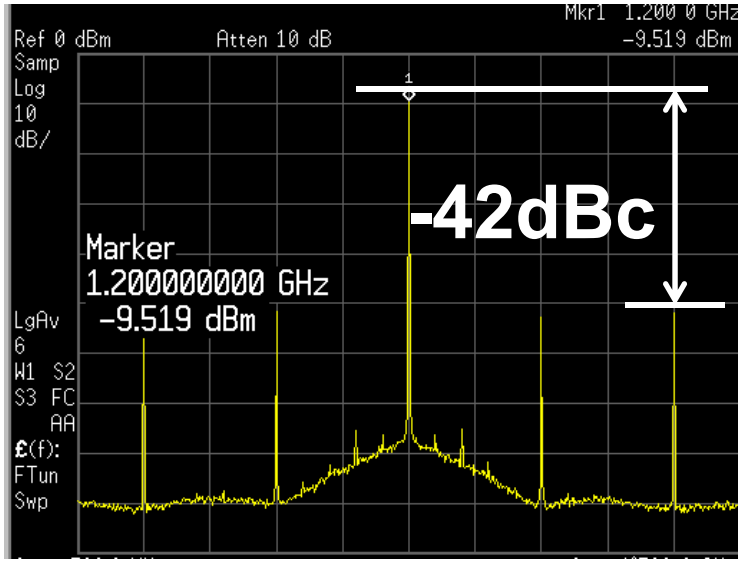


Phase Noise



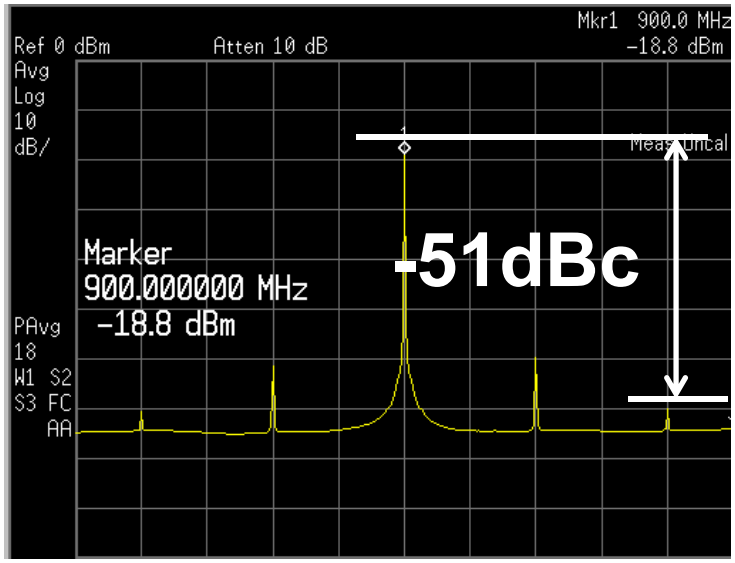
Measured Spur Level

Pulse Injection (Conventional) N=6



1st Spur: -41 dBc
2nd Spur: -42 dBc

Edge Injection (This work) N=6

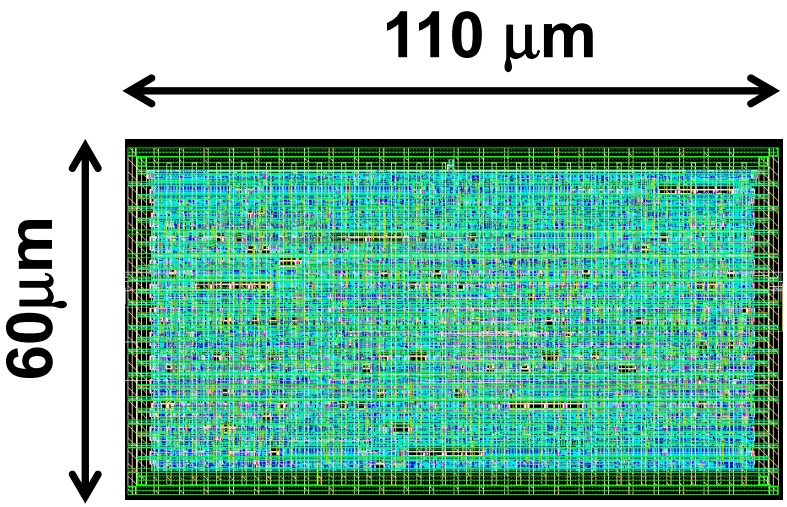


1st Spur: -41 dBc
2nd Spur: -51 dBc

N: Multiplication factor

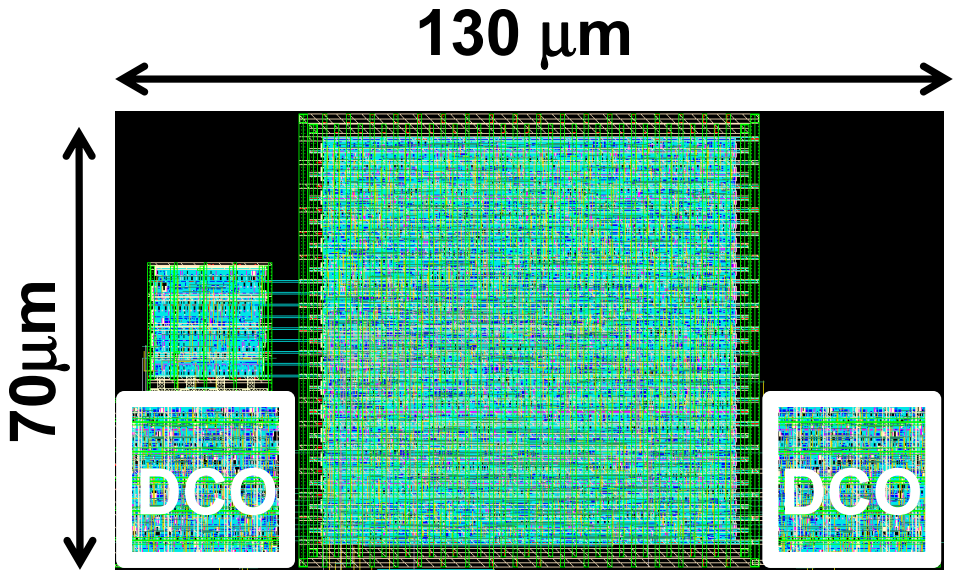
Layout Consideration

Integrating Jitter: 1.7ps
P_{DC}: 780μW
FOM: -236.5 dB



Fully synthesized (proposed)

Integrating Jitter: 2.32ps
P_{DC}: 640μW
FOM: -234.6 dB



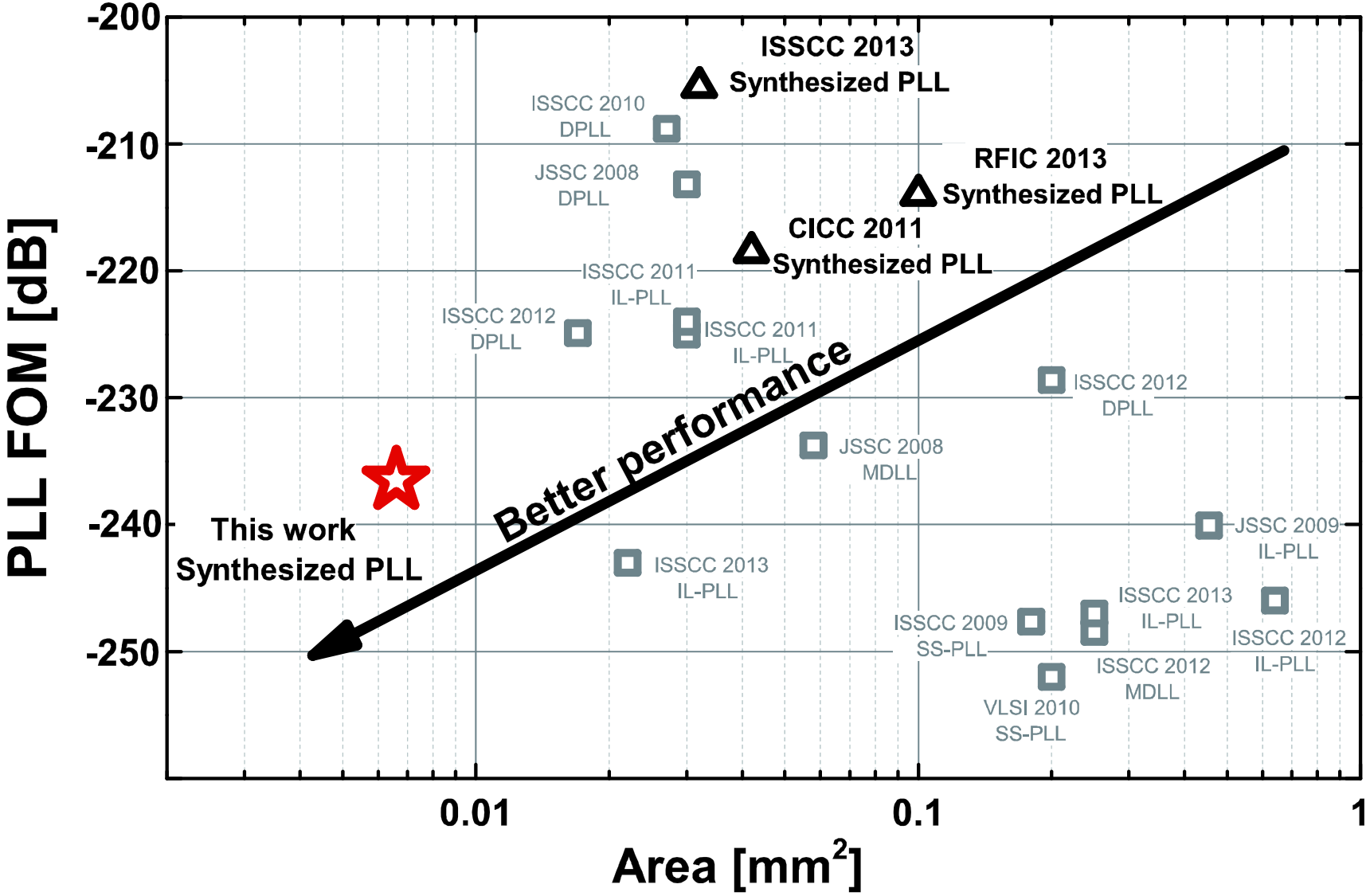
Hierarchical P&R with synthesized DCOs

Compar. of Synthesizable PLLs

	This work 65nm	[1] 28nm	[2] 65nm	[3] 65nm
Power [mW]	0.78 @900MHz	13.7 @2.5GHz	3.1 @250MHz	2.1 @403MHz
Area [mm^2]	0.0066	0.042	0.032	0.1
Integ. Jitter [ps]	1.7	N.A.	30	N.A.
RMS Jitter [ps]	2.8	3.2	N.A.	13.3
FOM [dB]	-236.5	-218.6*	-205.5	-214*
W/ custom cells?	No	No	Yes	Yes
Topology	IL-base	TDC-base	TDC-base	TDC-base

*FOM is calculated based on RMS jitter.

Performance Comparison



Conclusion

- **Synthesizable analog circuit design is proposed.**
  - By the digital design flow
  - Without any manual placement
  - Without any custom-designed cells
- **Fully synthesized PLL**
  - Dual-loop injection-lock topology
  - Current-output DAC
  - Ultra-fine frequency resolution
  - Interpolative-phase coupled oscillator

Acknowledgement

This work was partially supported by STARC, SCOPE, MIC, MEXT, Canon Foundation, and VDEC in collaboration with Synopsys, Inc., Cadence Design Systems, Inc., and Agilent Technologies Japan, Ltd.

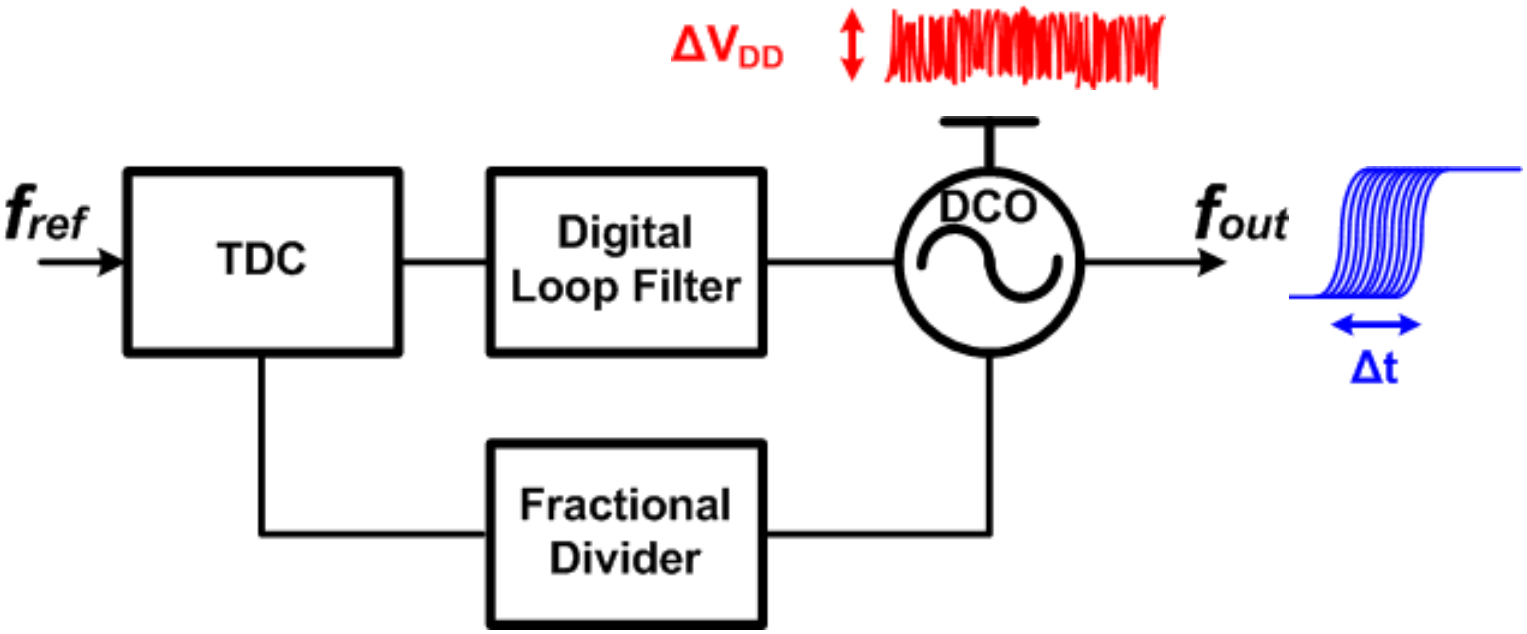
A 0.012mm^2 3.1mW Bang-bang Digital Fractional-N PLL with a Power Noise Cancellation Technique and a Walking-one Phase Selection Fractional Frequency Divider

Jenlung Liu, Tae-Kwang Jang, Yonghee Lee, Jungeun Shin, Seunghoon Lee, Taeik Kim, Jaejin Park, and Hojin Park

Samsung Electronics, Yongin, Korea

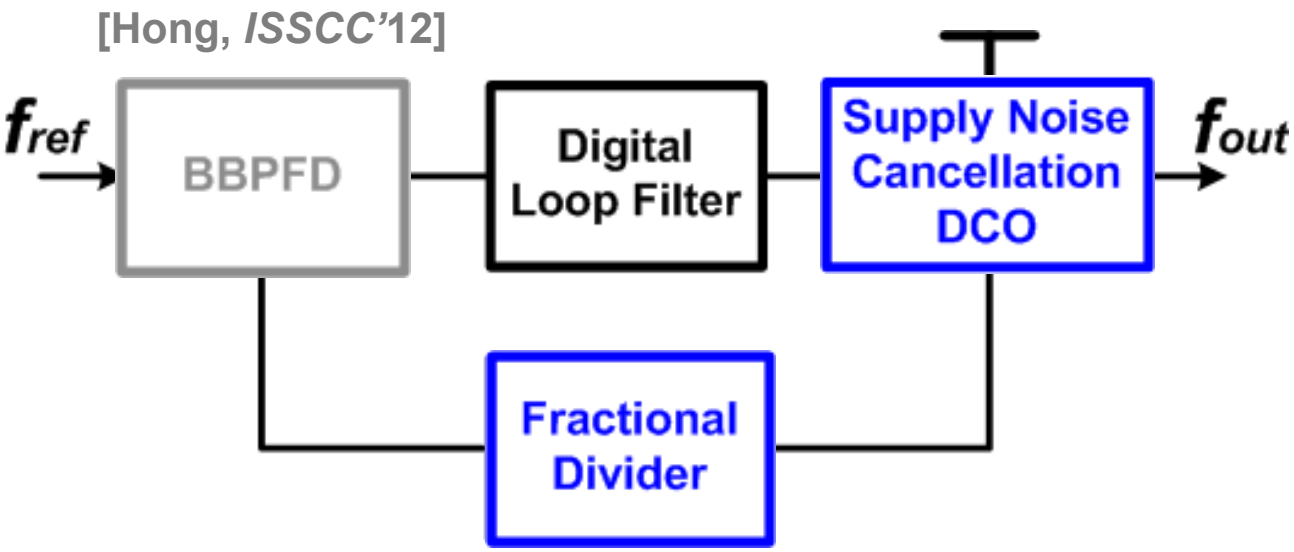
Two Issues in All-Digital Fractional-N PLL

- Power supply noise immunity
- Low power/area efficiency of digital PFD and fractional divider



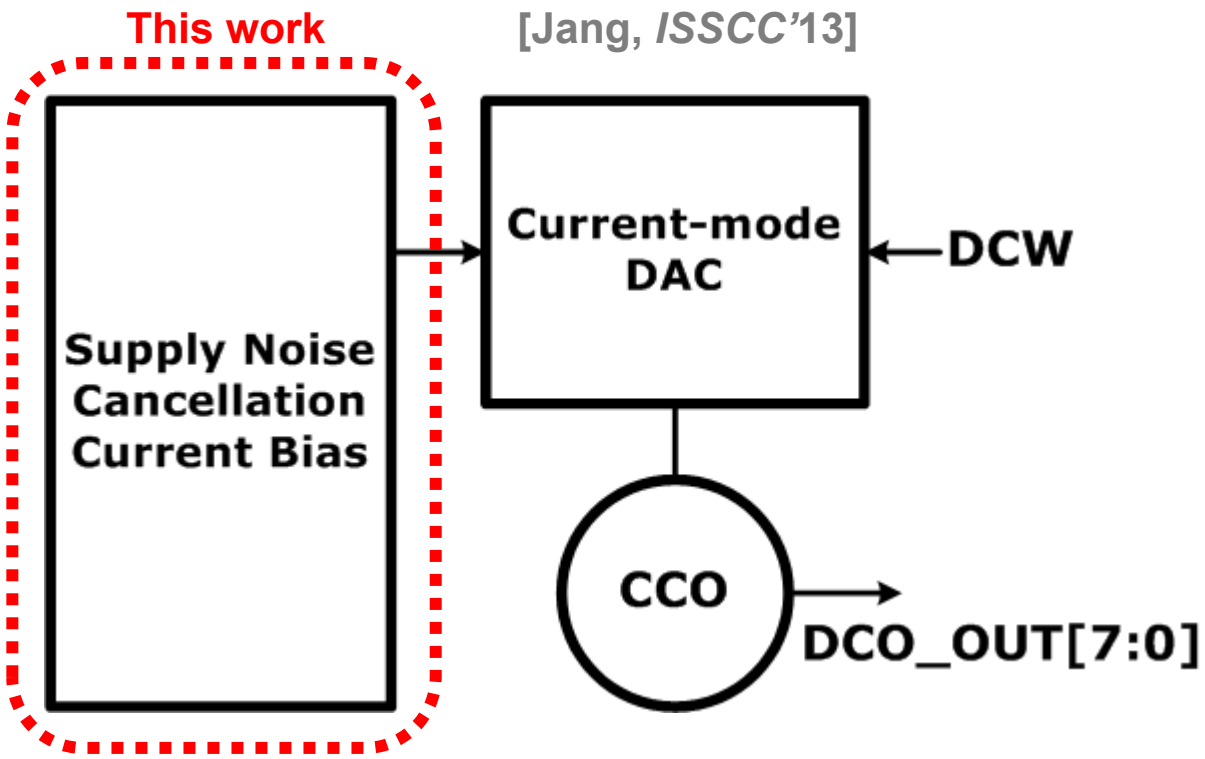
Proposed All-Digital Fractional-N PLL

- **Power supply insensitive DCO**
- **BBPFD instead of TDC**
- **Walking-one phase selector for a fractional divider**

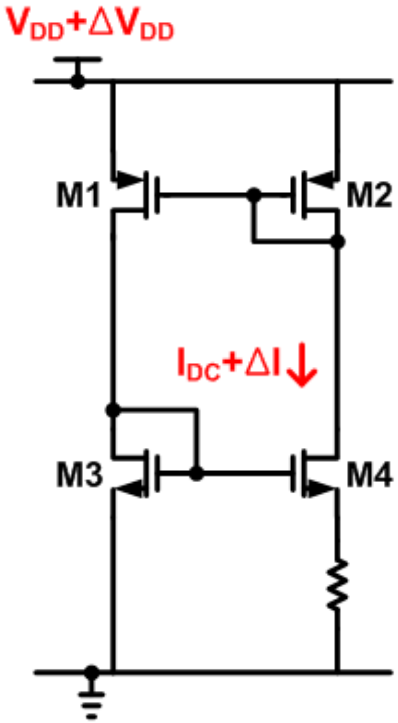


Proposed Supply Noise Cancellation Technique

- **Improved supply noise immunity by canceling noise in bias**



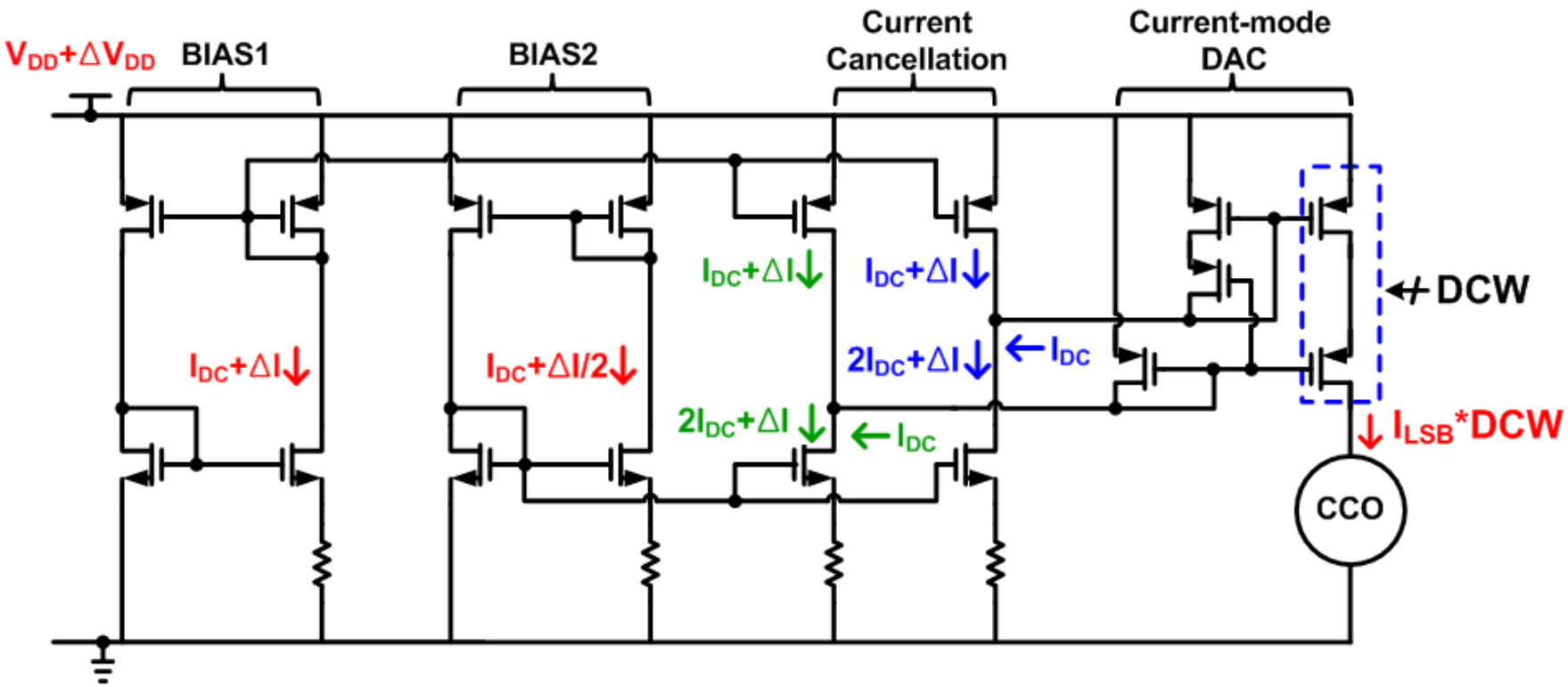
Constant-Gm Bias Current Generator



$$\frac{\Delta I}{\Delta V_{DD}} \approx \frac{1}{r_{o1}}\left[\frac{1}{2g_{m3}r_{o4}}+\frac{1}{2}\right]^{-1}$$

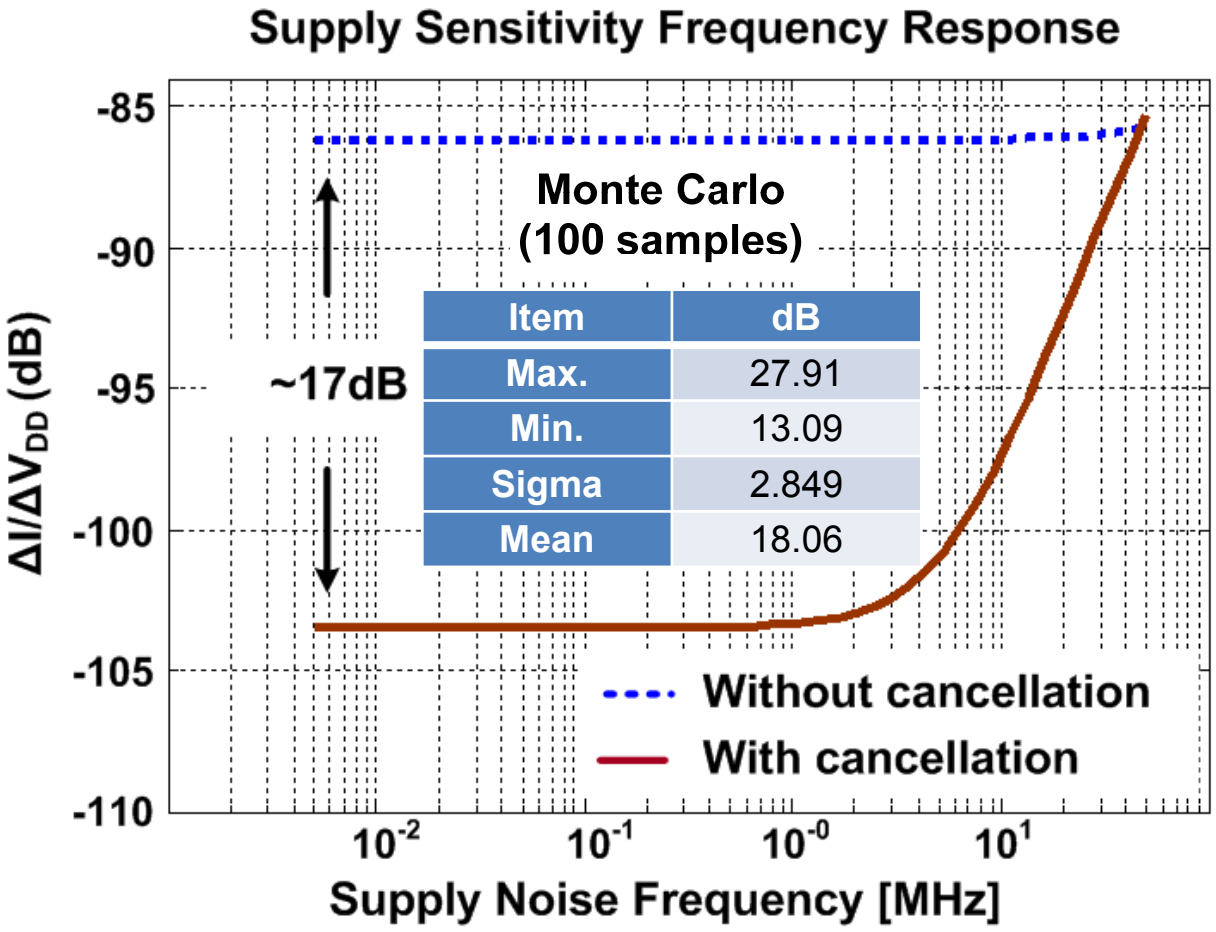
$$\propto \frac{1}{r_{o1}}$$

Supply Noise Cancellation



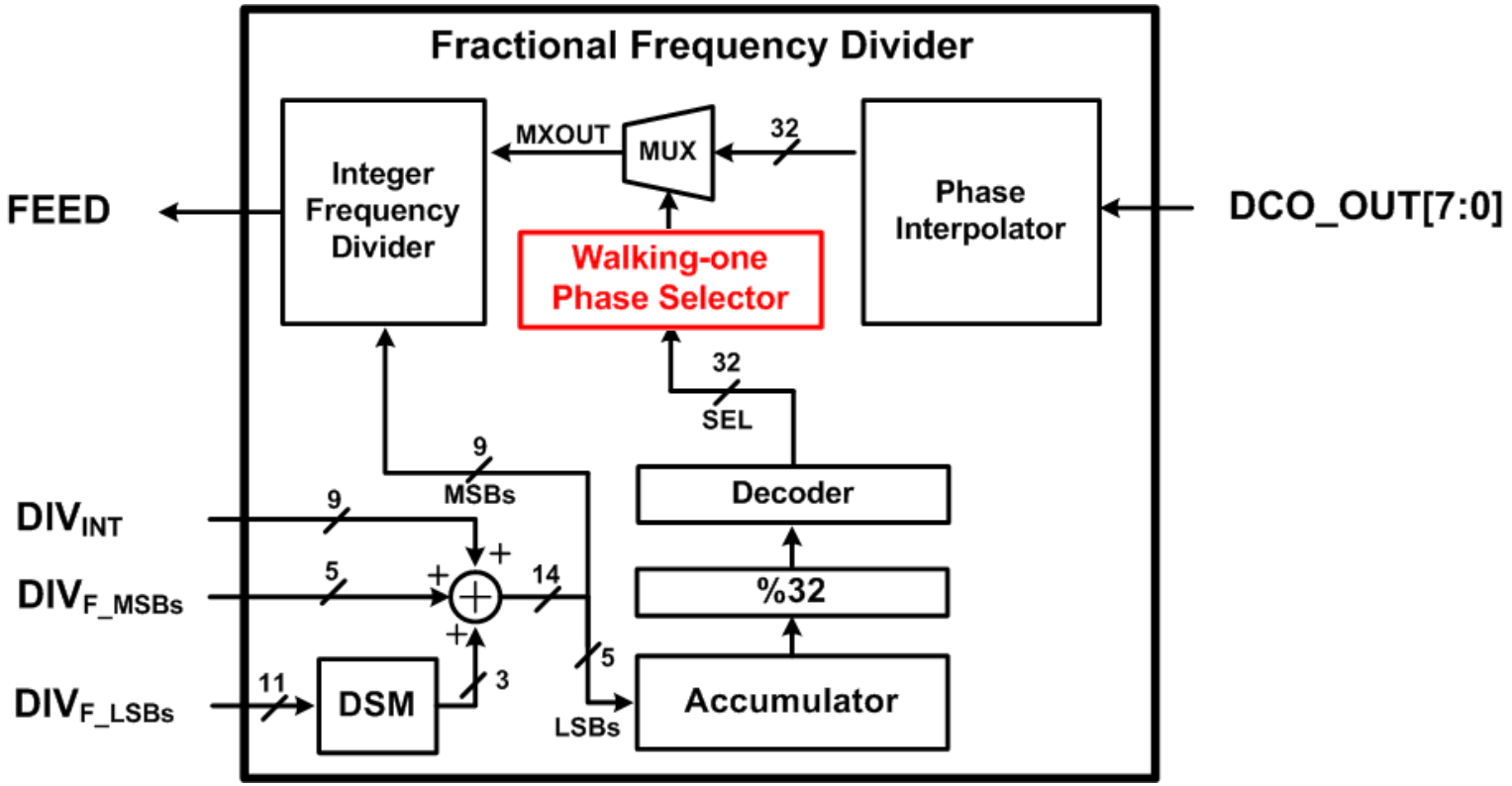
Simulated Supply Sensitivity

- 50mVpp sinusoid signal is added to a 0.9V DC supply



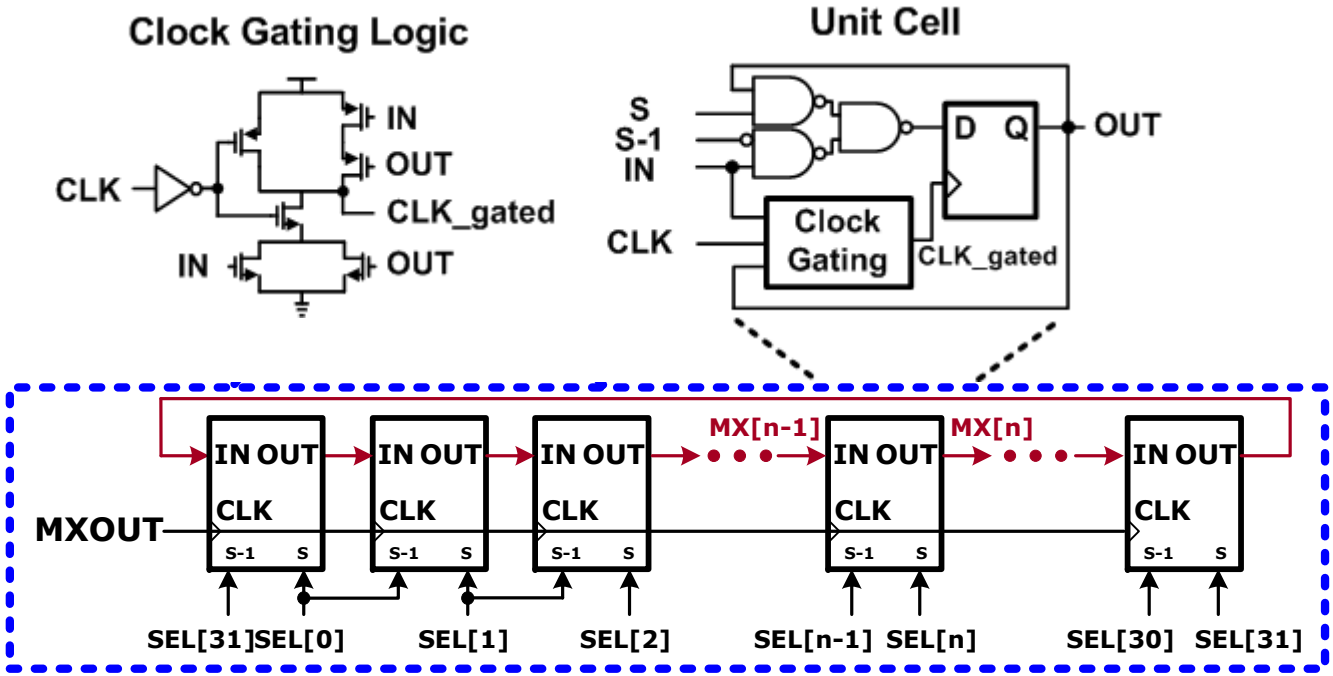
Fractional Divider Implementation

- Maximum phase dithering is reduced by a factor of 32
- A walking-one phase selector chooses target phase w/o glitches



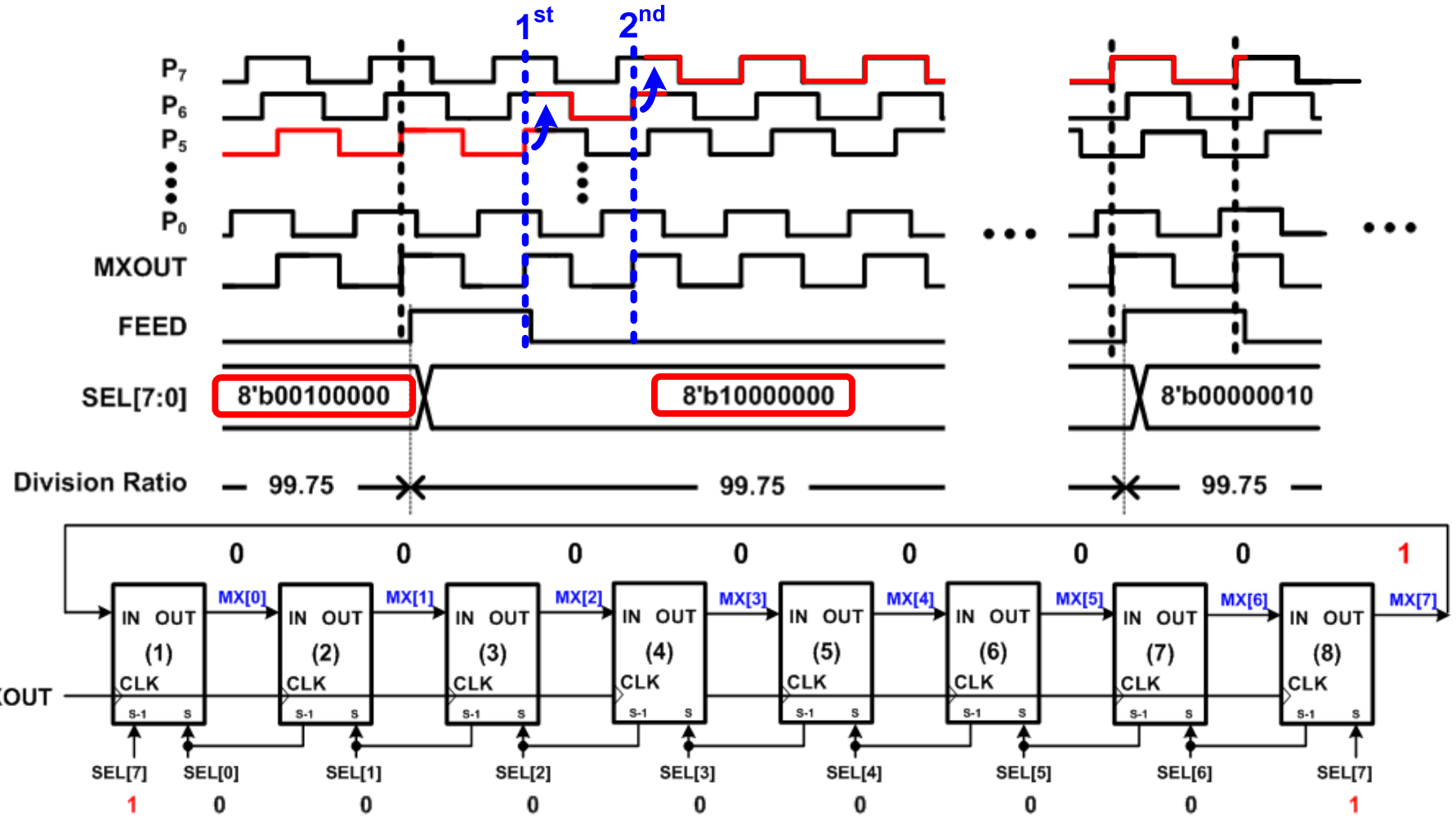
Walking-one Phase Selector

- Composed of a chain of 32 unit cells acting like DFFs
- Only one 1'b1 is travelling in the chain
- Controlling signals, S and S-1, decide whether 1'b1 propagates



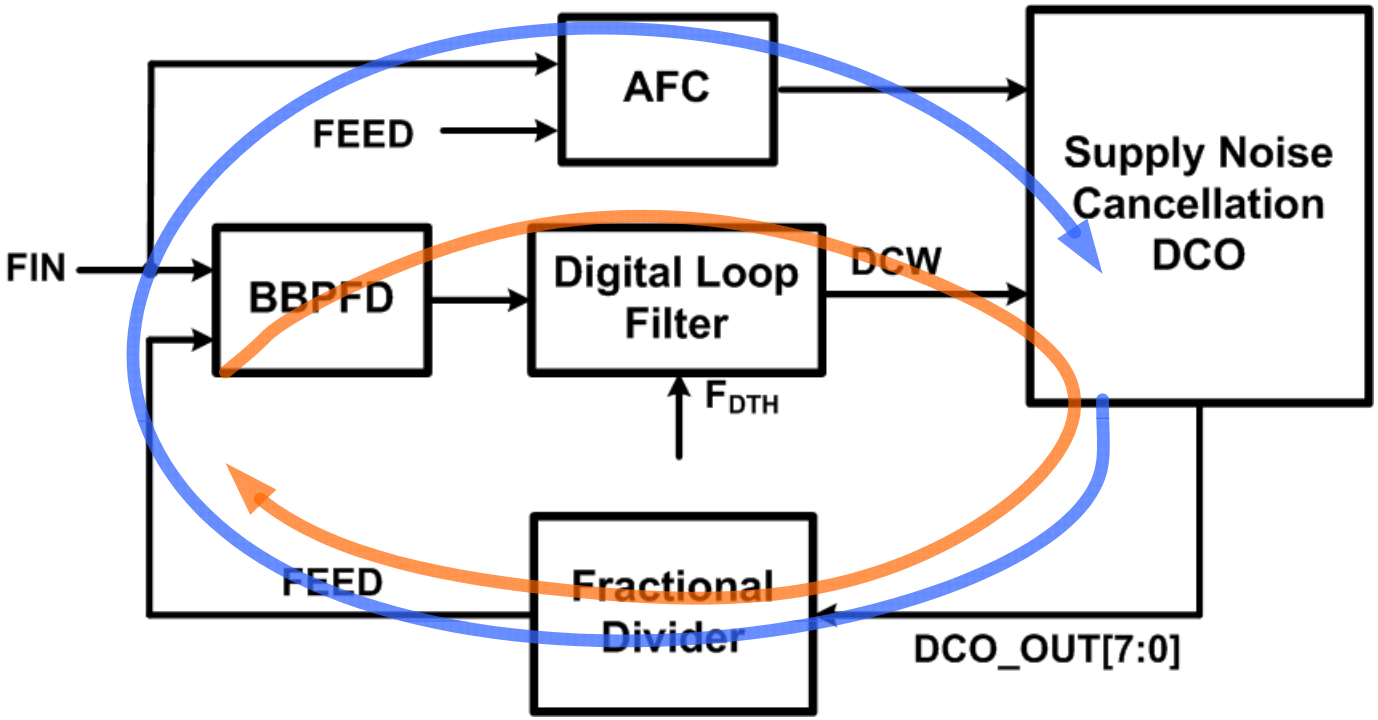
Walking-one Phase Selector Example

- 8-phase (P0 ~ P7) case with a division ratio of 99.75



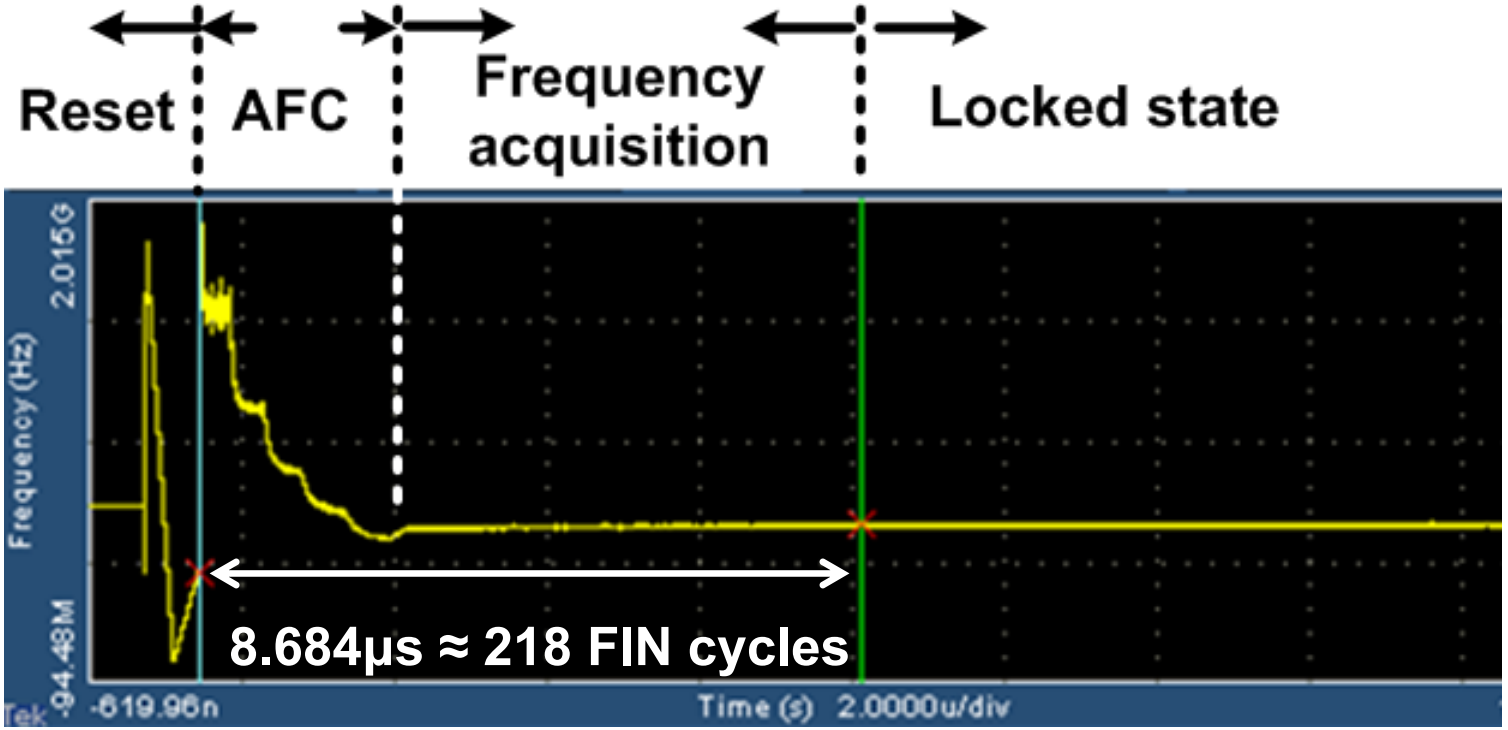
Top Functional Block Diagram

- Coarse tuning loop by AFC
- Fine tuning loop by BBPFD and digital loop filter

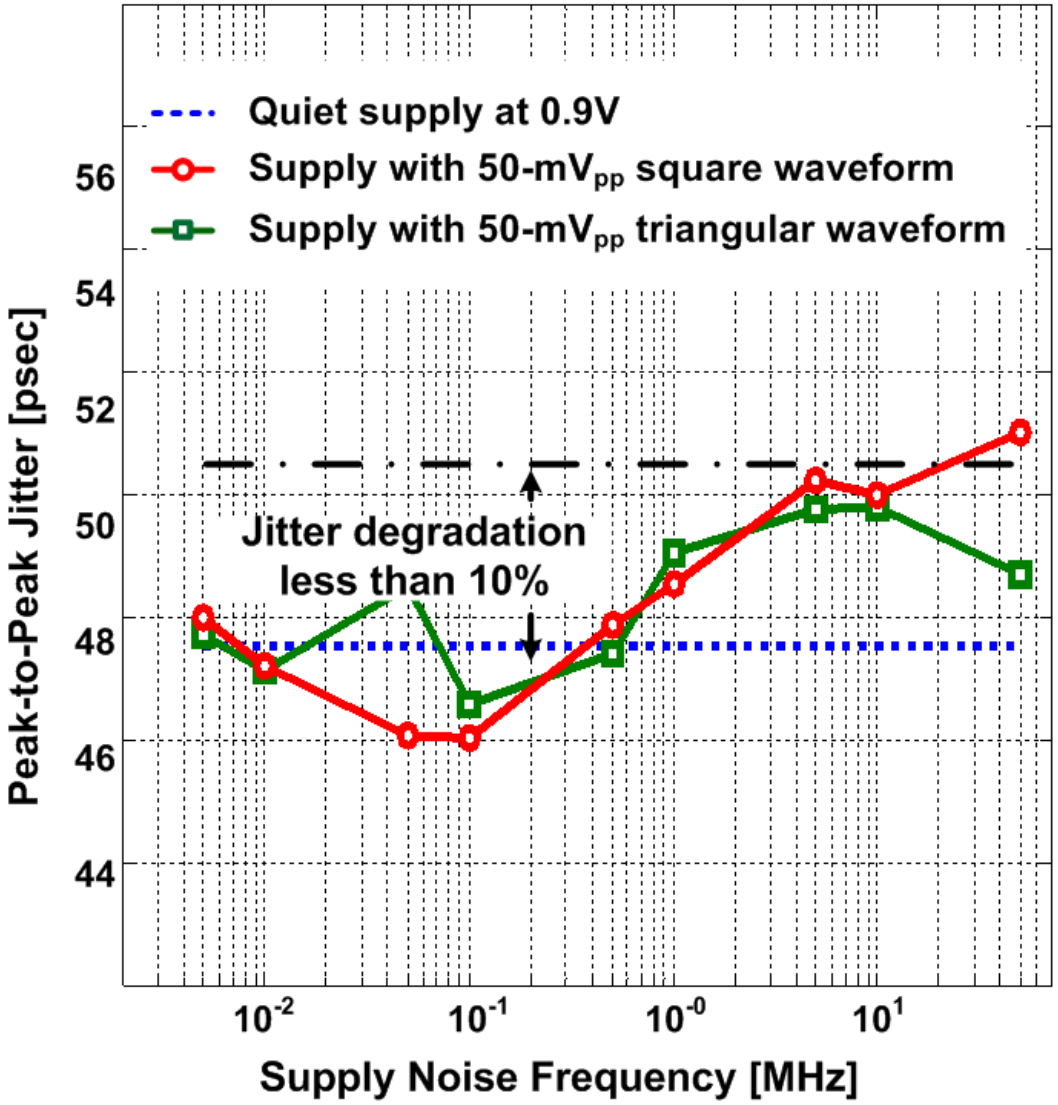


Frequency Time Trend Profile

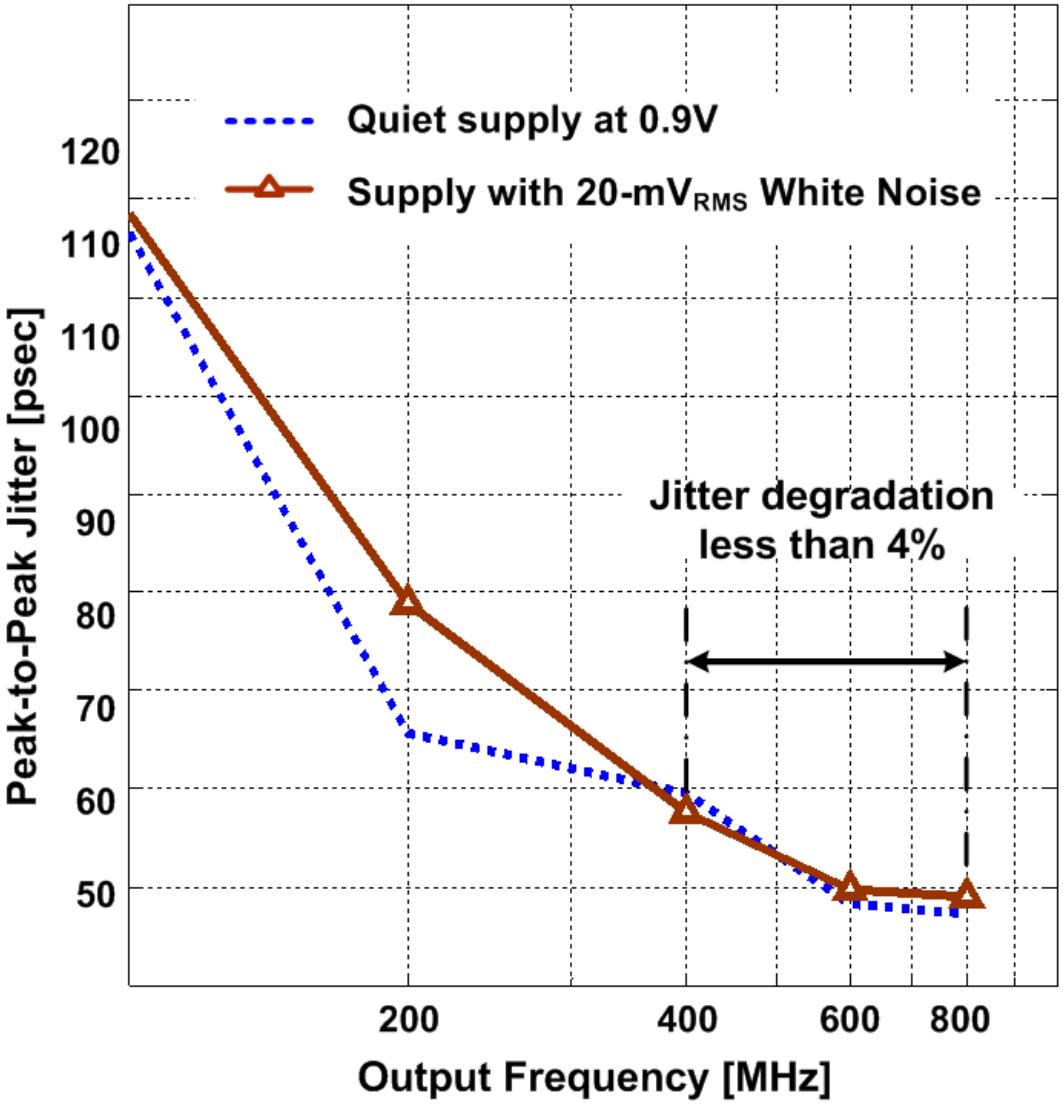
- Input /output frequency: 25MHz/600.1MHz



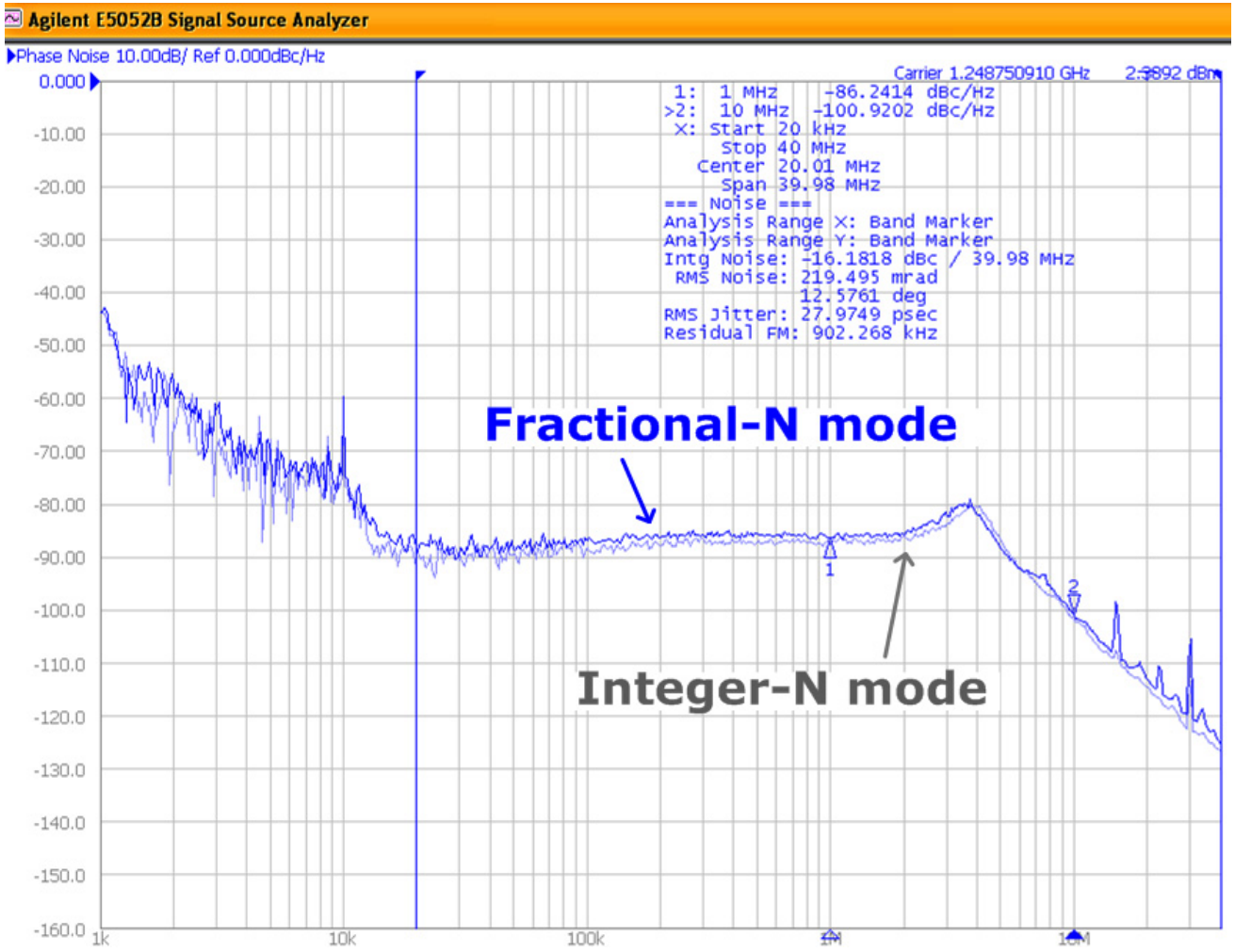
Jitter Performance under Supply Noise (1)



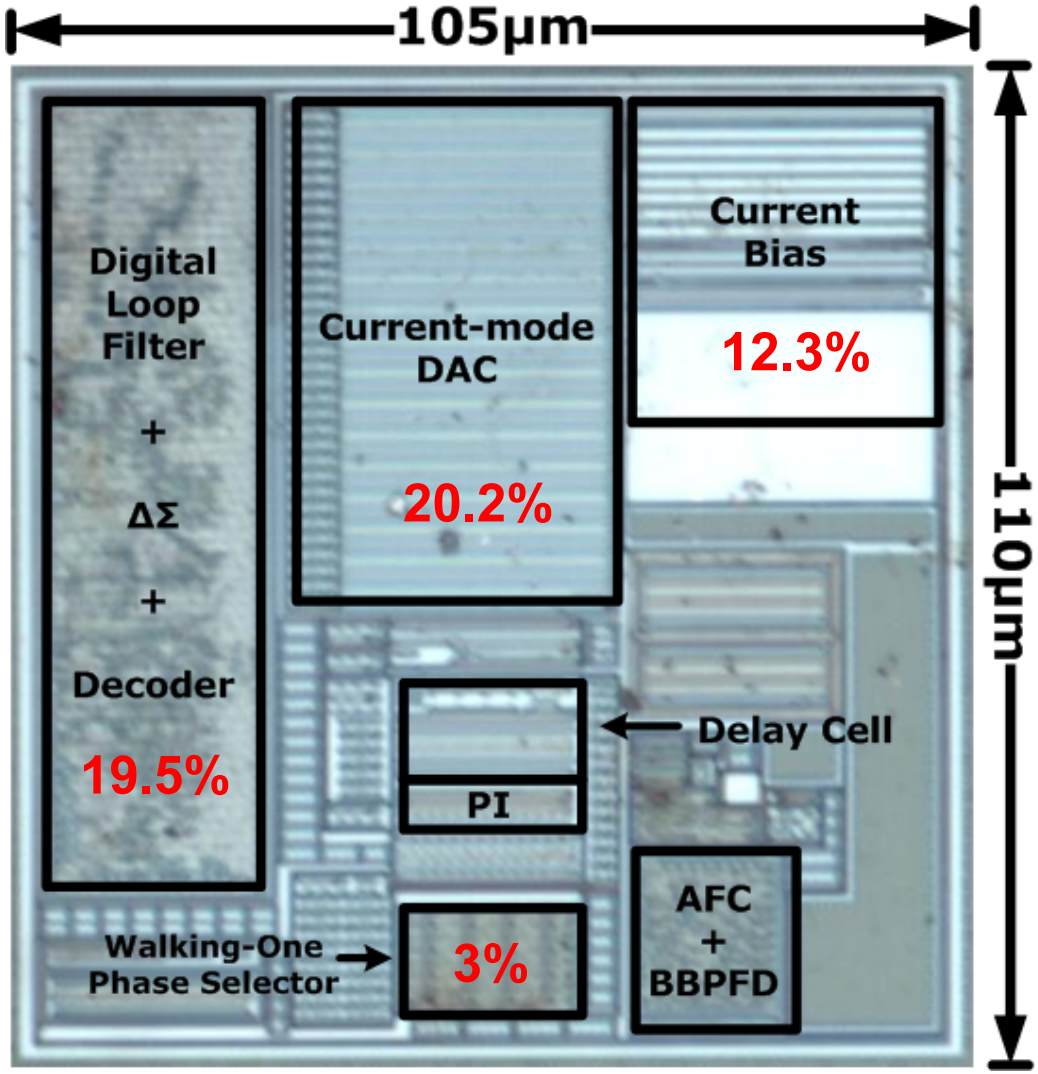
Jitter Performance under Supply Noise (2)



Phase Noise Measurement Result



Micrograph



Performance Summary

Technology	20nm		
Freq. Range [GHz]	0.025 – 1.6		
Output/DCO Freq. [GHz]	0.4/0.8	0.6/1.2	0.8/1.6
Period Jitter RMS/Pk-Pk [ps] — Quiet Supply	6.78/59.48	5.63/48.32	5.83/47.39
Period Jitter RMS/Pk-Pk [ps] — Supply with White Noise	7.08/57.57	6.20/49.67	5.89/49.87
Power [mW] — Analog	1.48	2.03	2.55
Power [mW] — Digital	0.28	0.43	0.55
Power [mW] — Total	1.76	2.46	3.10
Area [mm^2] — Analog	0.005		
Area [mm^2] — Digital	0.007		
Area [mm^2] — Total	0.012		

	This Work	ISSCC2013[4]	ISSCC2010[6]	JSSC2010[7]
Technology	20nm	28nm	65nm	130nm
Freq. Range [GHz]	0.025 - 1.6	0.032 - 2.0	0.6 - 0.8	0.3 - 1.4
Area [mm^2]	0.012	0.027	0.05	0.2
Power [mW]	3.1@1.6GHz	5.3@2.0GHz	3.2@0.8GHz*	16.5@1.35GHz
Normalized Power [mW/GHz]	1.94	2.65	4	12.22
Jitter (RMS) [ps]	4-7 / 28**	19.3	20-30	3.7

* Assuming 1.2V supply

** Period jitter / integrated jitter

Conclusion

- *The digital fractional-N PLL with low power-supply-noise sensitivity is implemented in 20nm CMOS process*
- *The small-area power-supply-noise-cancelling scheme is introduced*
- *The fractional divider with a walking-one phase selector reduces design complexity, power consumption, and die area*
- *The proposed digital PLL occupies 0.012mm² and consumes 3.1mW at 1.6GHz*

Reference

[1] A. Rylyakov, *et al.*, "*Bang-Bang Digital PLLs at 11 and 20GHz with Sub-200fs Integrated Jitter for High-Speed Serial Communication Applications*," *ISSCC Dig. Tech. Papers*, pp. 94-95, 2009.

[2] A. Elshazly, *et al.*, "*A 0.4-to-3GHz Digital PLL with Supply-Noise Cancellation using Deterministic Background Calibration*," *ISSCC Dig. Tech. Papers*, pp. 92-94, 2011.

[3] R.B. Staszewski, *et al.*, "*All-Digital PLL and Transmitter for Mobile Phones*," *IEEE J. Solid-State Circuits*, pp. 2469-2482, vol40, no. 12, Dec. 2005.

[4] T-K. Jang, *et al.*, "*A 0.026mm^2 5.3mW 32-to-2000MHz Digital Fractional-N Phase Locked-Loop using a Phase-Interpolating Phase-to-Digital Converter*," *ISSCC Dig. Tech. Papers*, pp. 254-255, 2013.

[5] R. Nonis, *et al.*, "*A 2.4psrms-jitter Digital PLL with Multi-Output Bang-Bang Phase Detector and Phase-Interpolator-Based Fractional-N Divider*," *ISSCC Dig. Tech. Papers*, pp. 356-357, 2013.

[6] M. S.W. Chen, *et al.*, "*A Calibration-Free 800MHz Fractional-N Digital PLL with Embedded TDC*," *ISSCC Dig. Tech. Papers*, pp. 472-473, 2010.

[7] D.S. Kim, *et al.*, "*A 0.3–1.4 GHz All-Digital Fractional-N PLL With Adaptive Loop Gain Controller*," *IEEE J. Solid-State Circuits*, pp. 2300-2311, vol. 45, no. 11, Nov. 2010.

A 2.4GHz ADPLL with Digital-Regulated Supply-Noise-Insensitive and Temperature-Self-Compensated Ring DCO

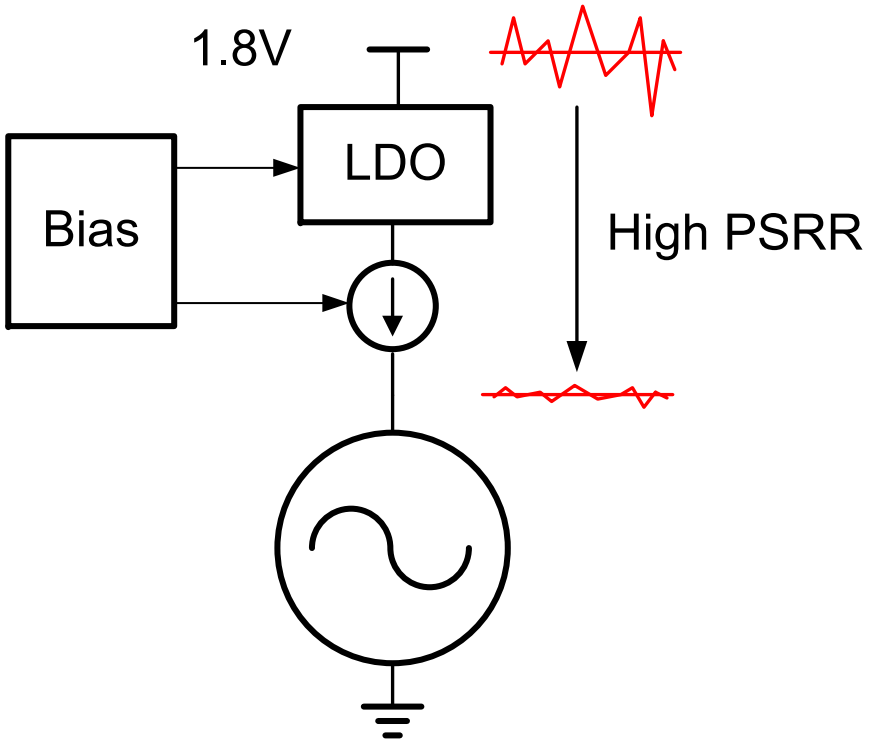
Yi-Chieh Huang, Che-Fu Liang, Hsien-Sheng Huang, and Ping-Ying Wang

MediaTek, Hsinchu, Taiwan

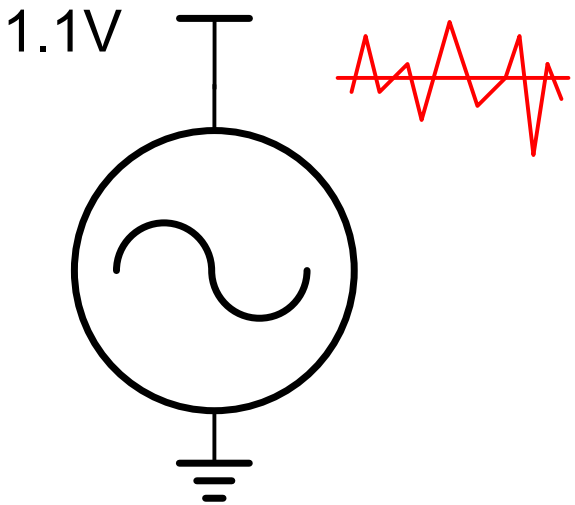
Agenda

- Motivation
- Proposed Structure
- Measurement Results
- Conclusion

Motivation(1/2)



$$Pushing = \frac{dfreq}{dV}$$



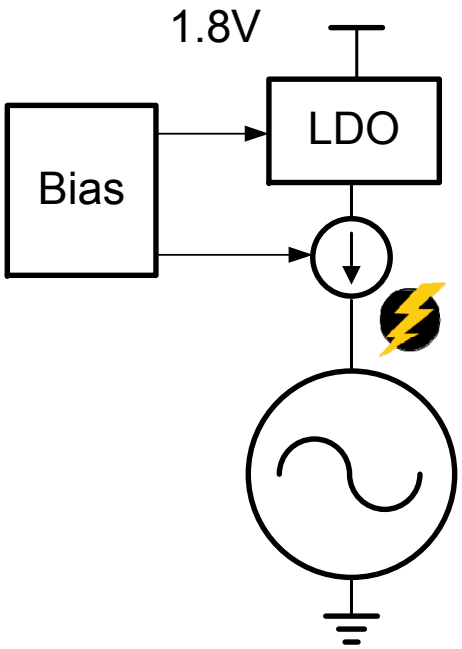
$$\frac{dfreq}{dV}\Delta V = \Delta freq$$

5GHz/V 0

$$\frac{dfreq}{dV}\Delta V = \Delta freq$$

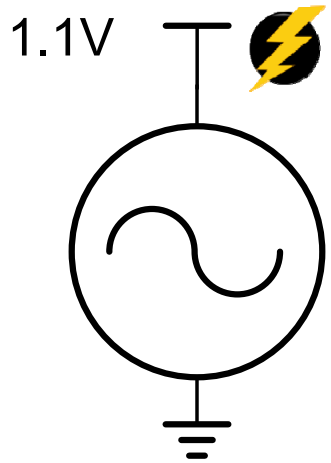
0 10mV

Motivation(2/2)



$$\frac{dfreq}{dV}\Delta V = \Delta freq$$

5GHz/V

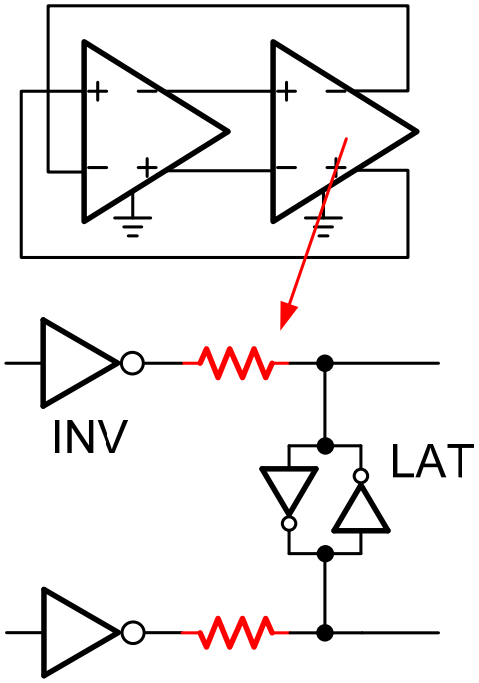


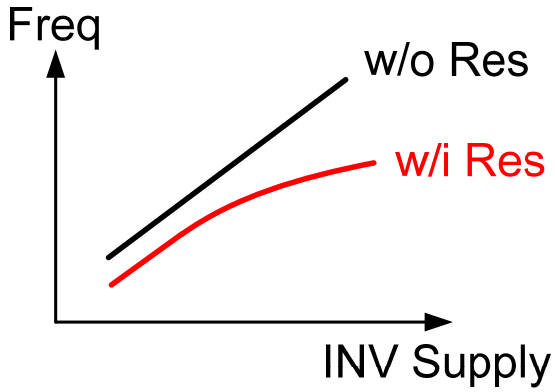
$$\frac{dfreq}{dV}\Delta V = \Delta freq$$

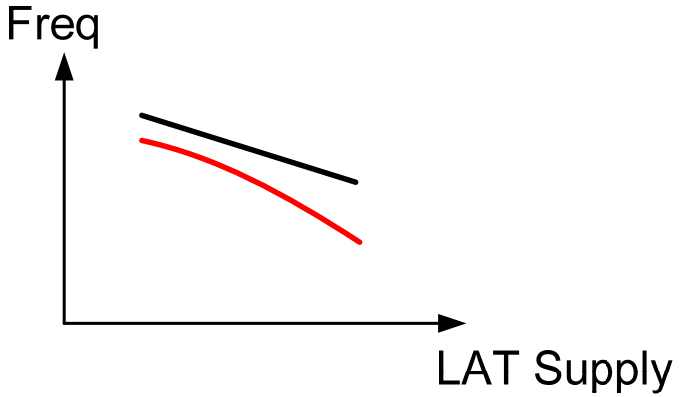
0

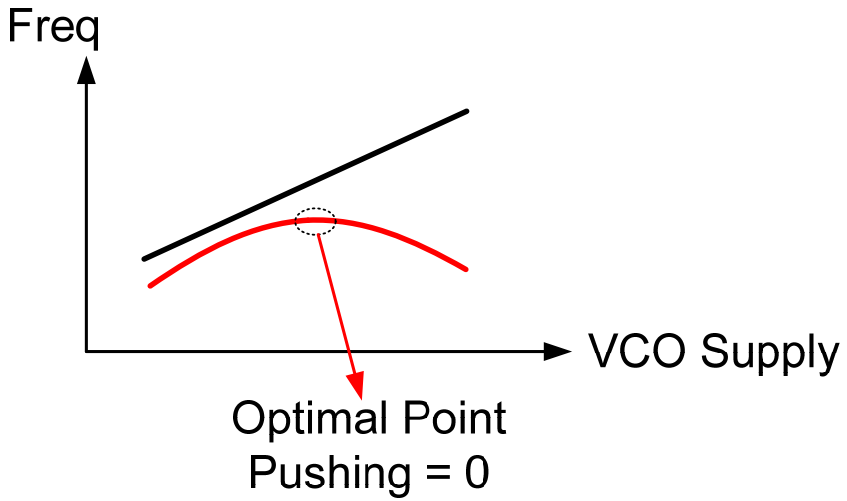
- Unexpected noise immunity

Proposed VCO



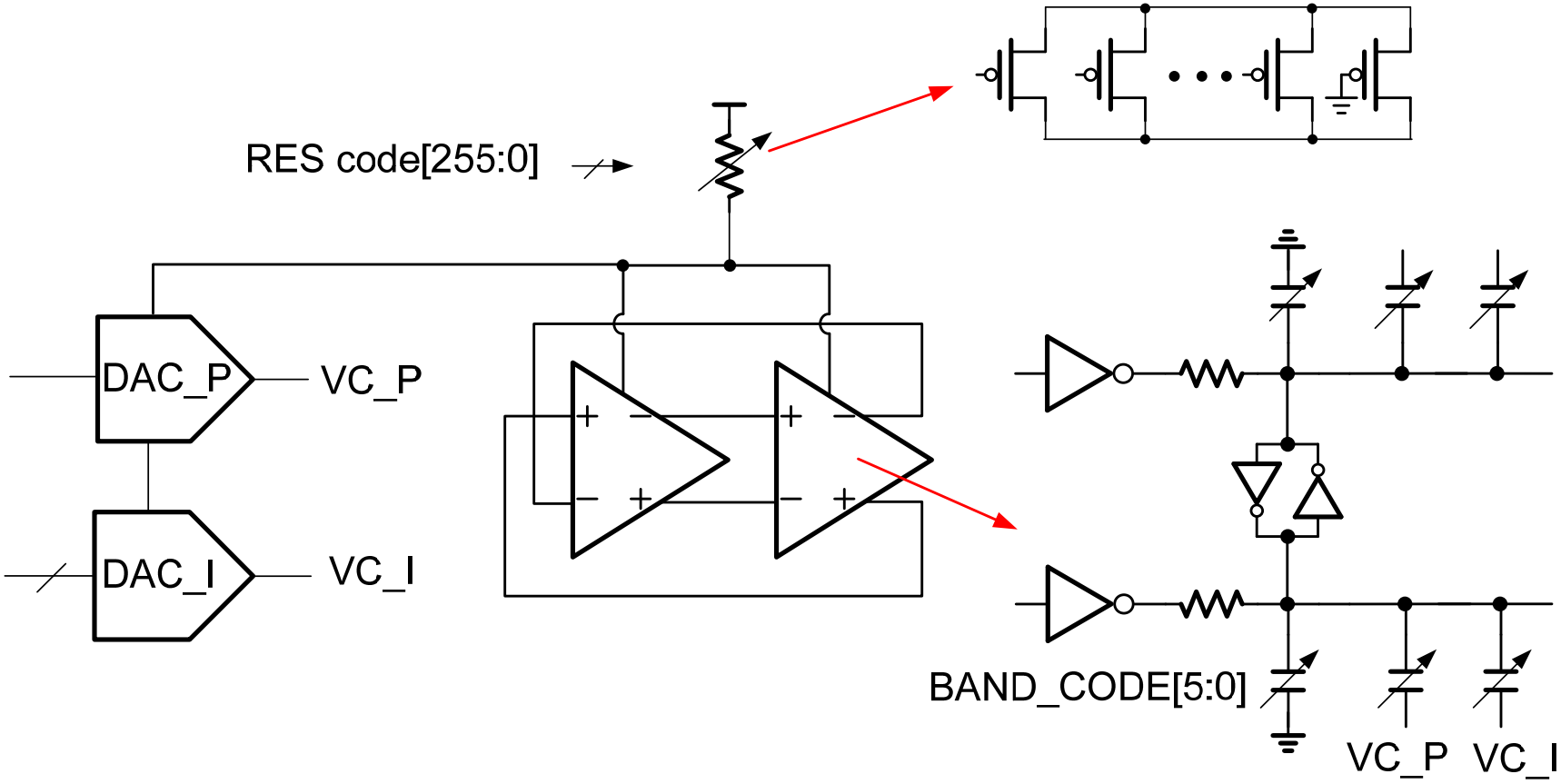






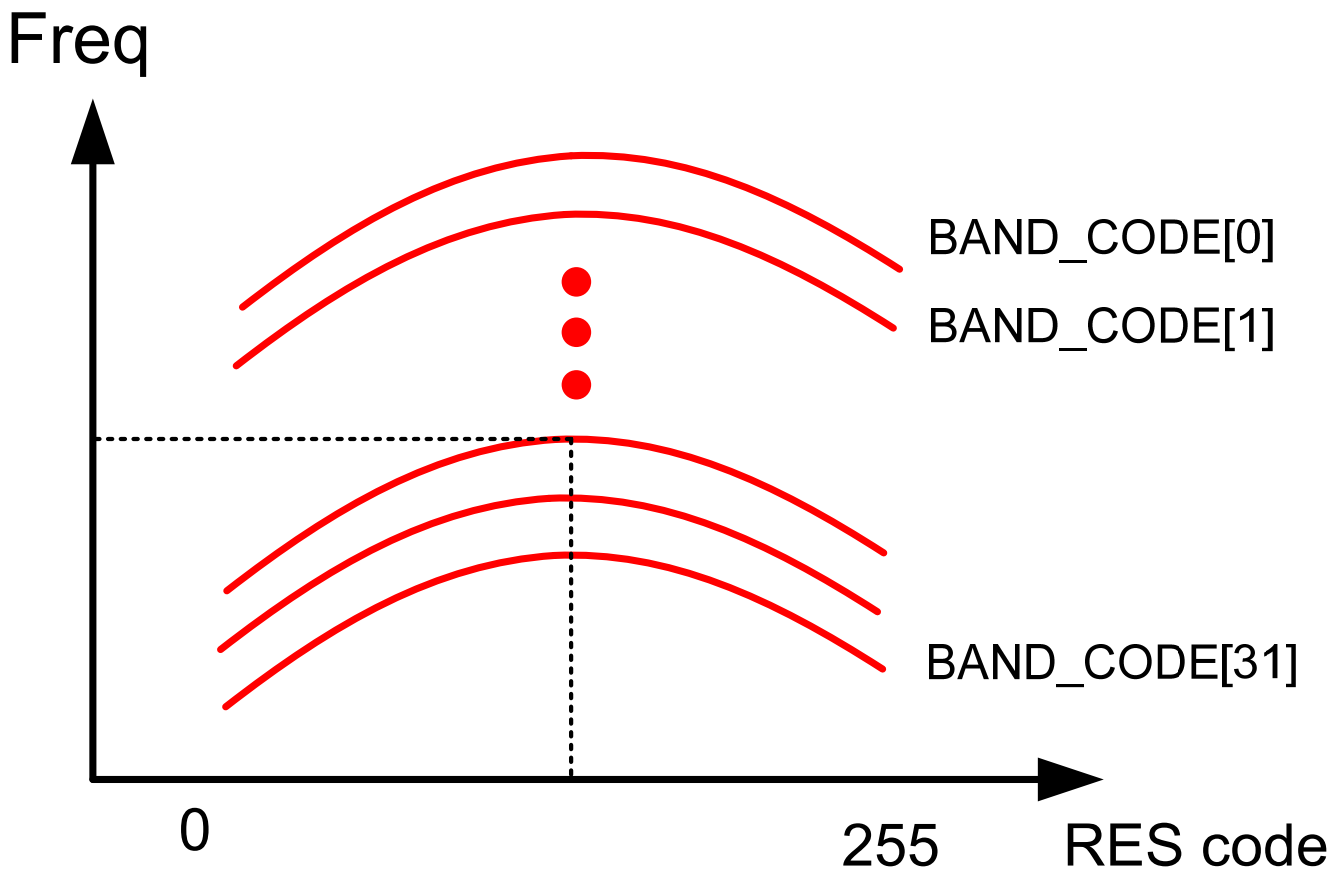
- Resistor desensitizes VCO pushing
- Calibration is needed

DCO



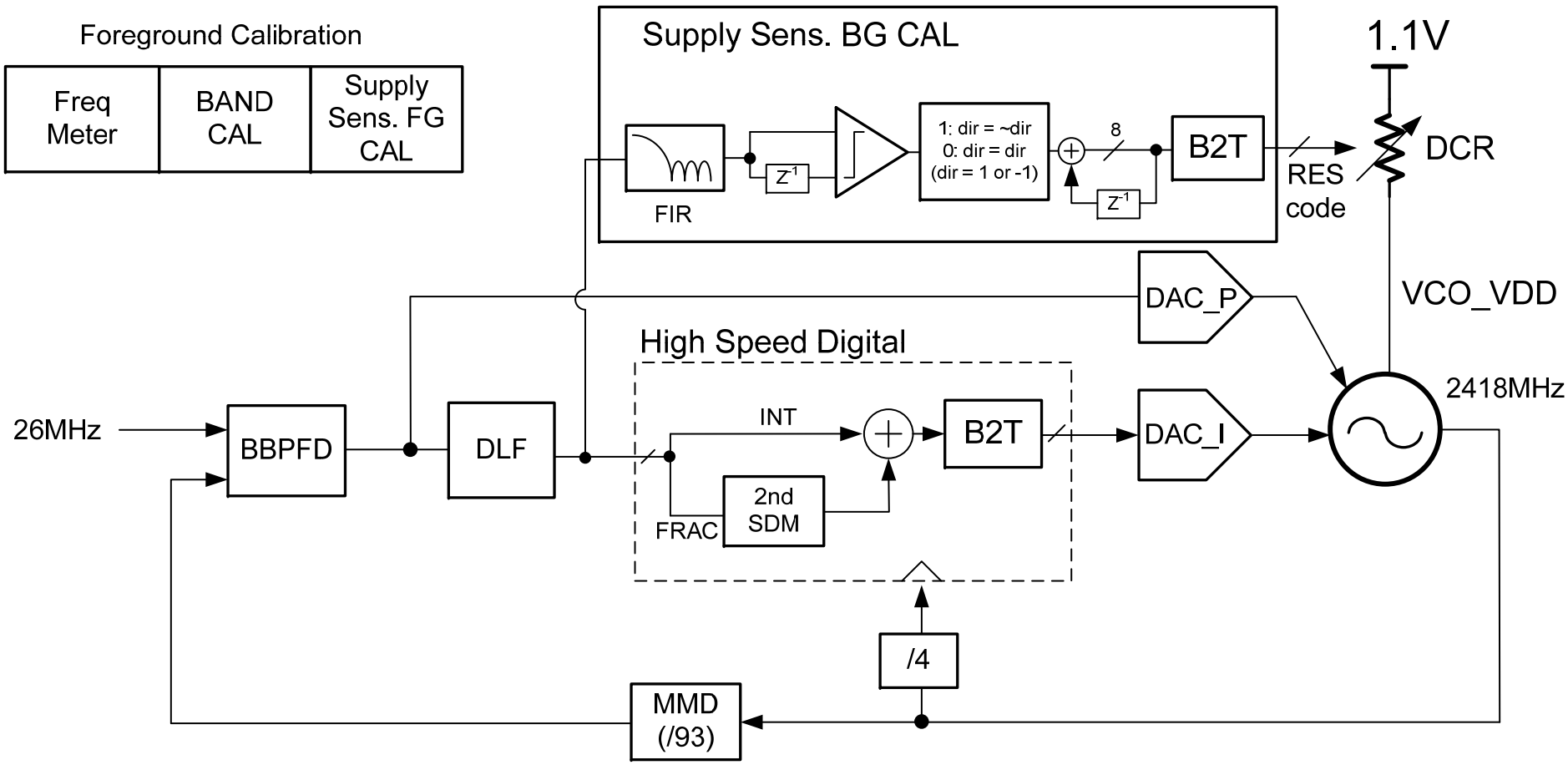
- No LDO, current source and bias
- Digital-regulated VCO supply
- Low supply voltage

Frequency/Pushing Calibration



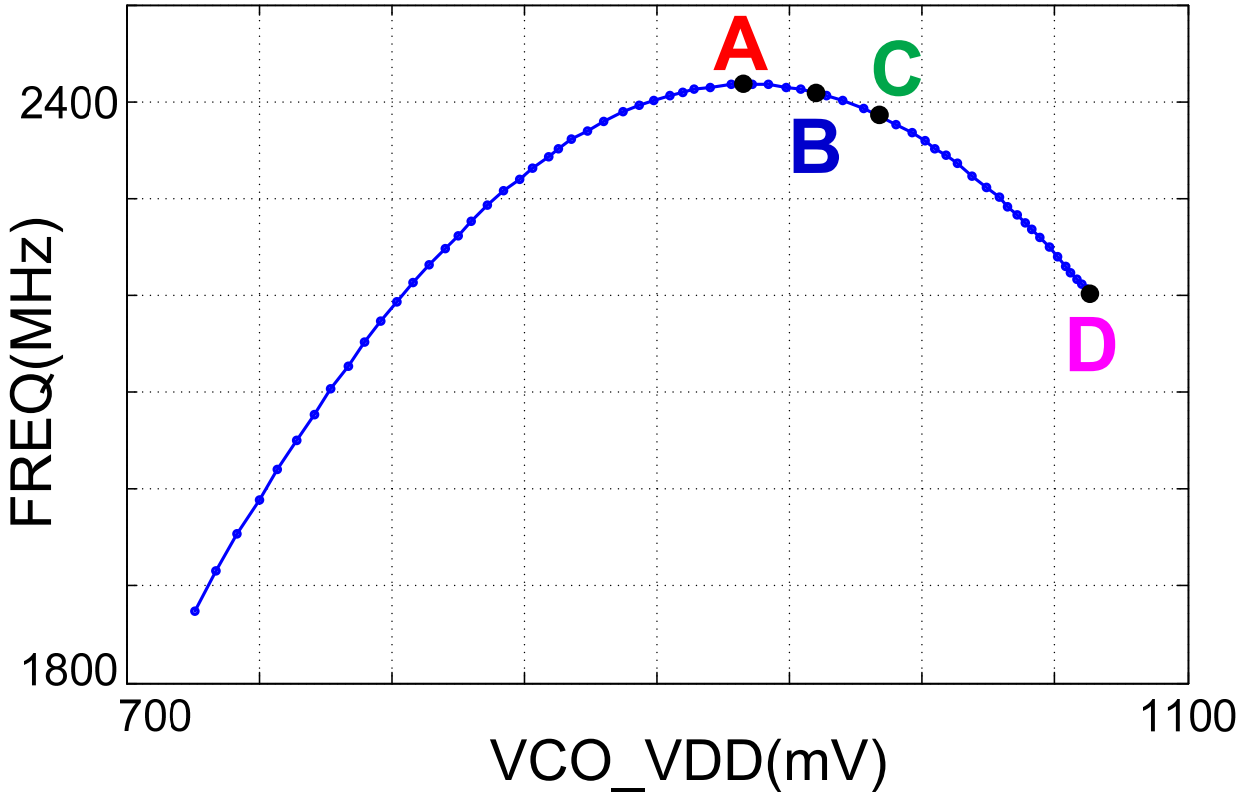
- Step 1 : Search for optimal supply insensitive point
- Step 2 : Search for designed frequency

Proposed ADPLL



- DLF is monitored to regulate VCO supply

Measured FREQ V.S. VDD

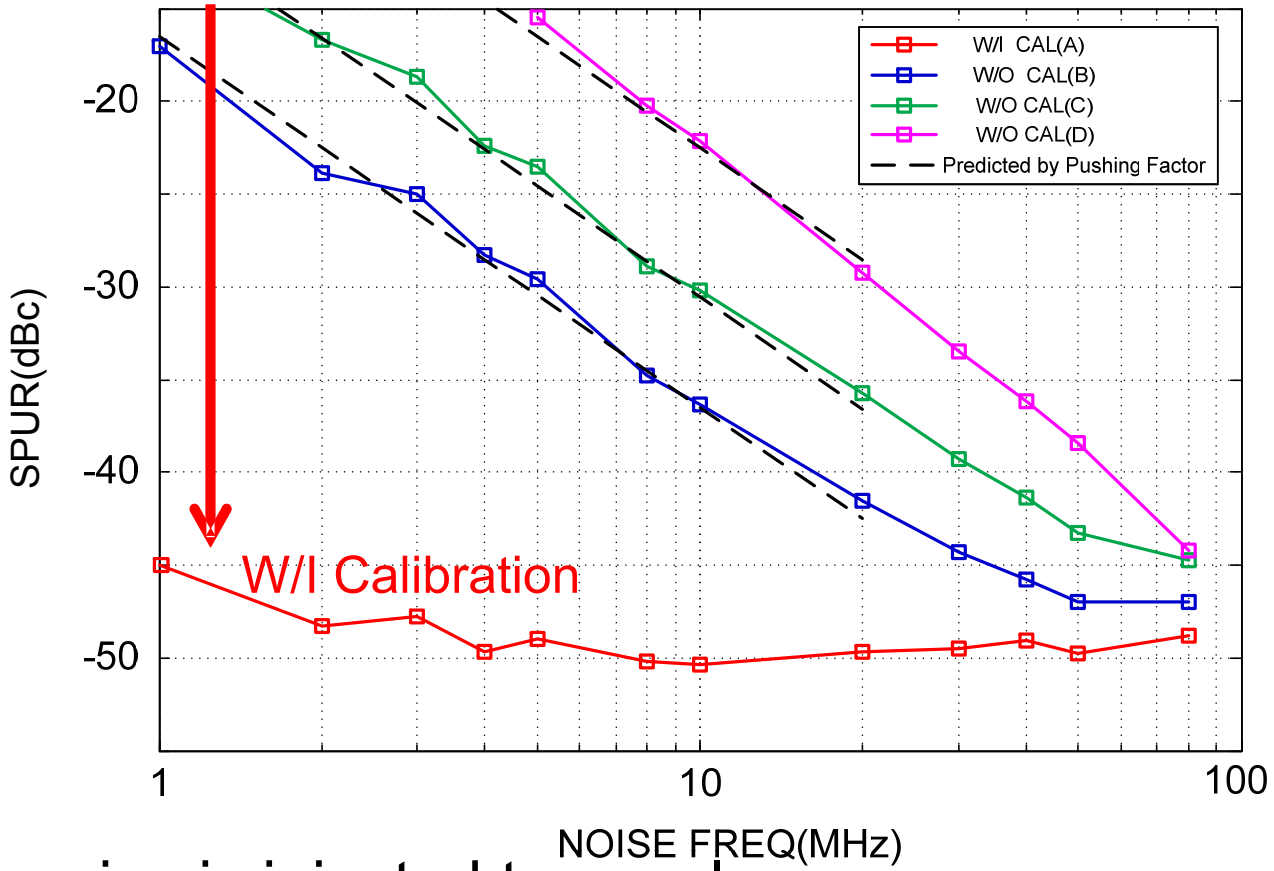


VCO_VDD	A	B	C	D
Pushing	22.5MHz/V	600MHz/V	1186MHz/V	3000MHz/V

- >100x Improvement, equivalent to 42.5dB PSRR

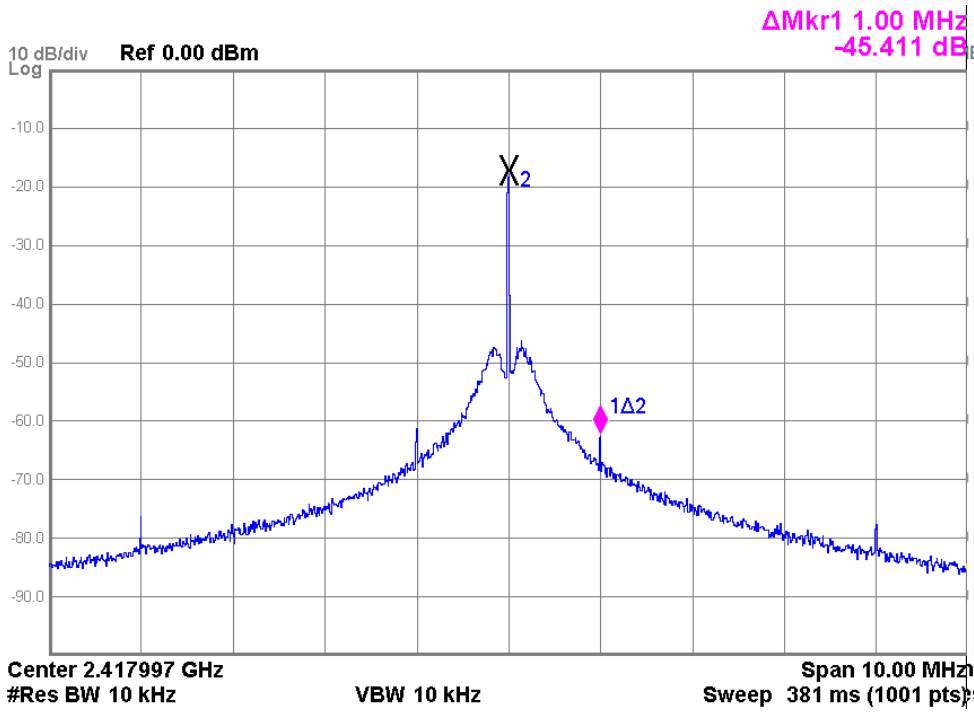
Dynamic Supply Sensitivity Test(1/2)

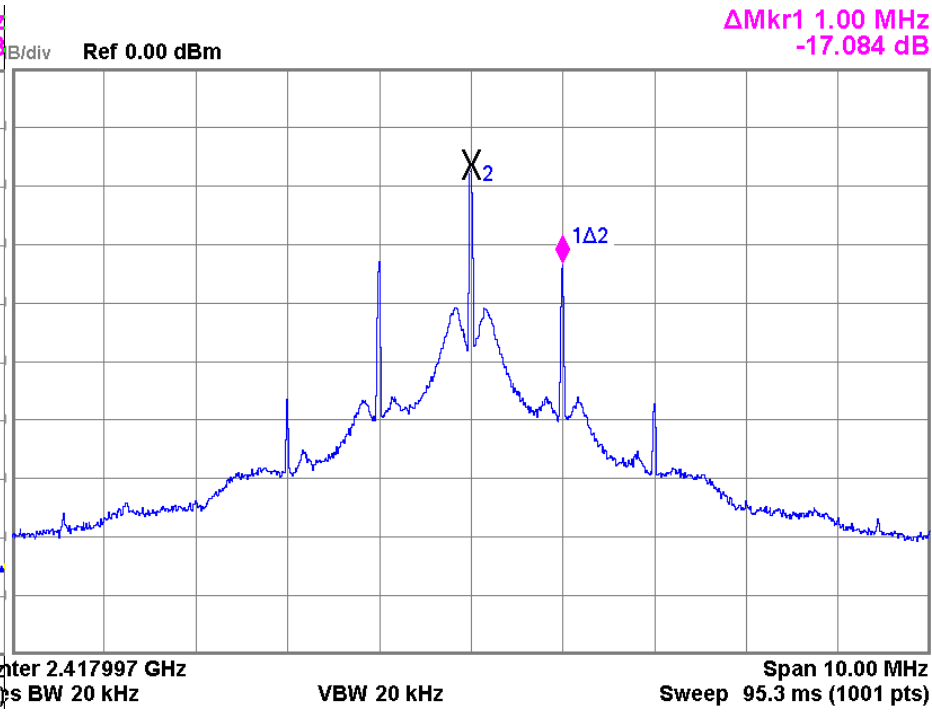
$$Spur = 20\log\left(\frac{Amp \cdot Pushing}{2 \cdot Noise\_Freq}\right)$$



- 1mVpp noise is injected to supply
- PLL BW<<1MHz

Dynamic Supply Sensitivity Test(2/2)

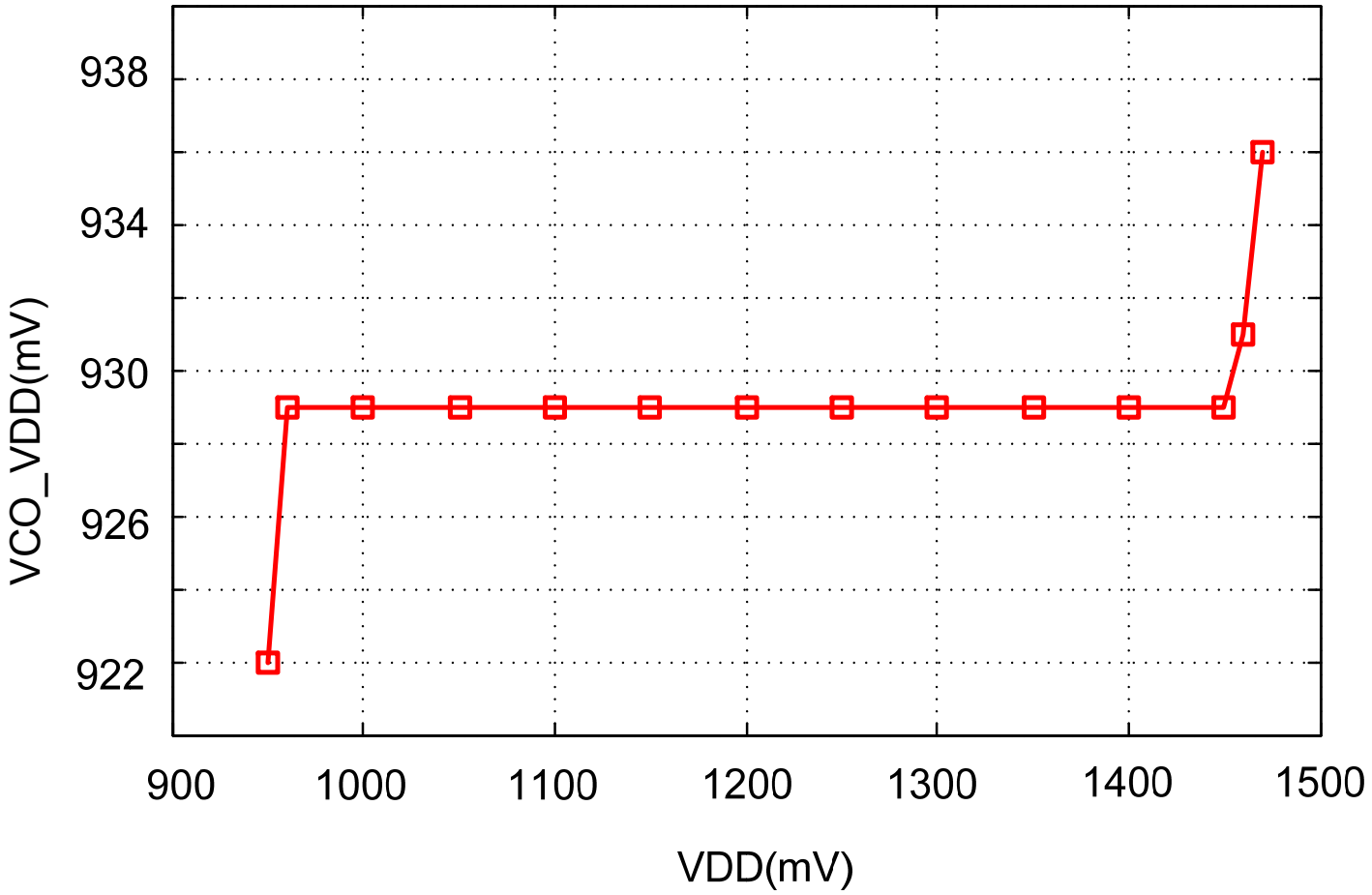




Pushing =22.5MHz/V

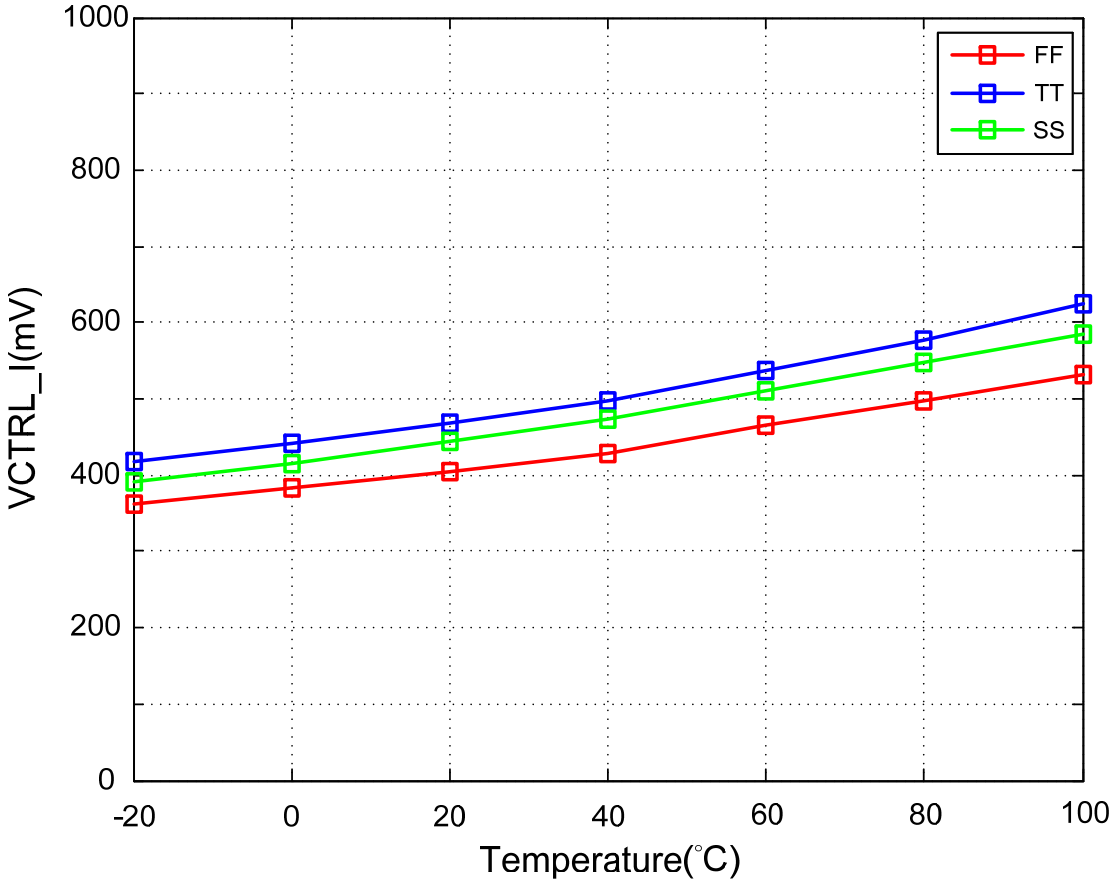
Pushing =600MHz/V

Static Supply Sensitivity Test



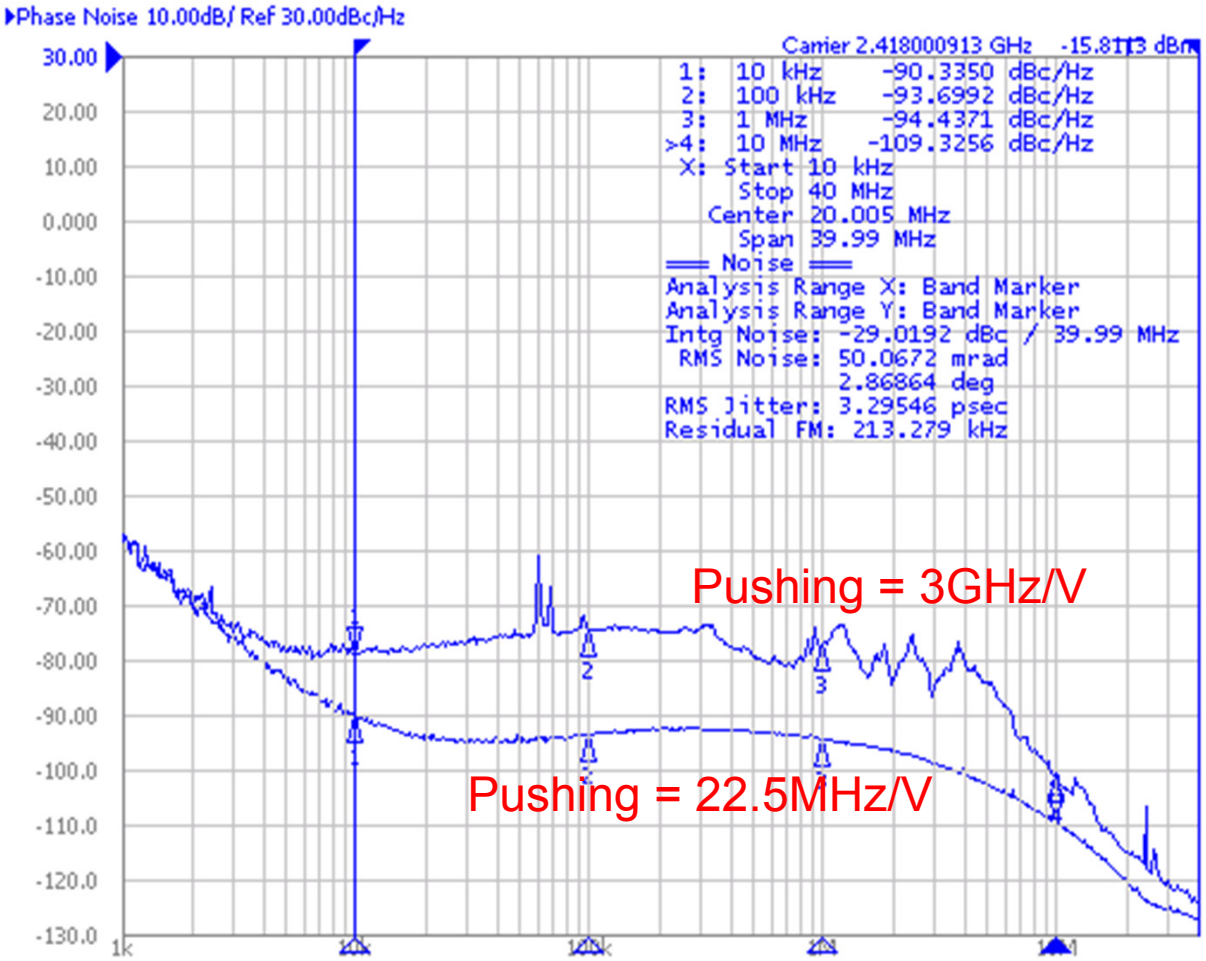
- Optimal supply insensitive point is tracked by calibration loop

Measured Frequency Drift over Temperature



- As pushing= 0, temperature coefficient is compensated
- Simulation ~1%, Measurement ~2% variation
- Kvco = 250MHz/V

Phase Noise Measurement



- >20dB Phase noise improvement
- RMS jitter = 3.29ps

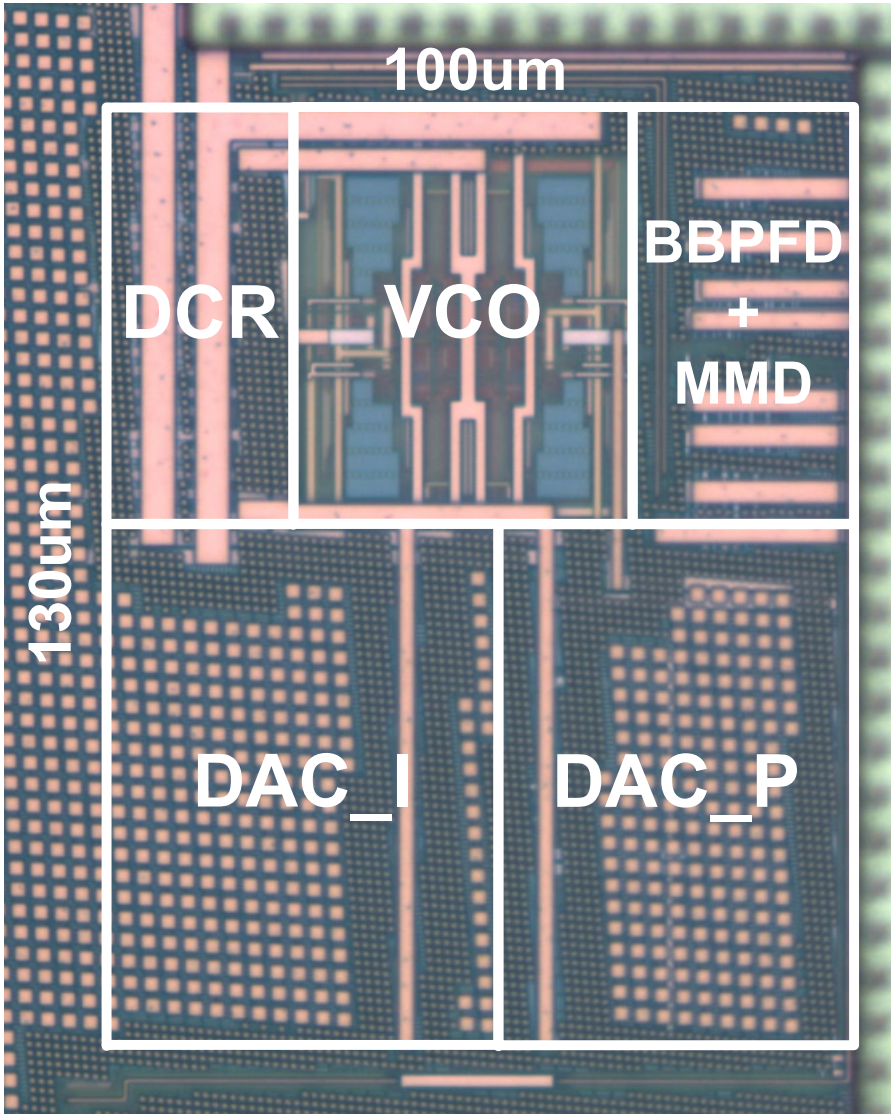
Performance Summary

	JSSC03 [5]	JSSC07 [4]	JSSC09 [3]	ISSCC11 [2]	JSSC12 [1]	This Work
Technology	0.25um	130nm	65nm	130nm	90nm	40nm
Supply	2.5	1.0	1.1	1.1	1.0	1.1
Ref CK(MHz)	250	N/A	1280	N/A	N/A*	26
Fosc(MHz)	1000	1400	5120	2500	5650	2418
RMS Jitter(ps)	3.28	3.9	1.56	4.6	N/A*	3.29
Power(mW)	10	9.6	39.7	3.1	7~26**	6.4
Supply Sensitivity	0.03	N/A	0.0077	N/A	0.019	0.0087
Calibration	No	Foreground Calibration	No	Background Calibration	No	Background Calibration

*VCO only **operate at 0.63~8.1GHz

Technology	40nm
Supply	1.1
Power	Analog 4.2mW Digital 2.2mW Total 6.4mW
RMS Jitter(10kHz~40MHz)	3.29ps
Supply Sensitivity	0.0087
Pushing Factor	22.5MHz/V
Reference Spur	-75dBc
Frequency Drift(-20~100°C)	2%

Die photo



Summary

- Remove analog LDO/current source/bias
- Realize low supply/power/pushing VCO
- Low frequency variation over temperature
- Background loop guarantees robustness

A 20-to-1000MHz ±14ps Peak-to-Peak Jitter Reconfigurable Multi-Output All-Digital Clock Generator Using Open-Loop Fractional Dividers in 65nm CMOS

Ahmed Elkholy[1], Amr Elshazly[2], Saurabh Saxena[1], Guanghua Shu[1], and Pavan Kumar Hanumolu[1]

[1]University of Illinois, Urbana, IL

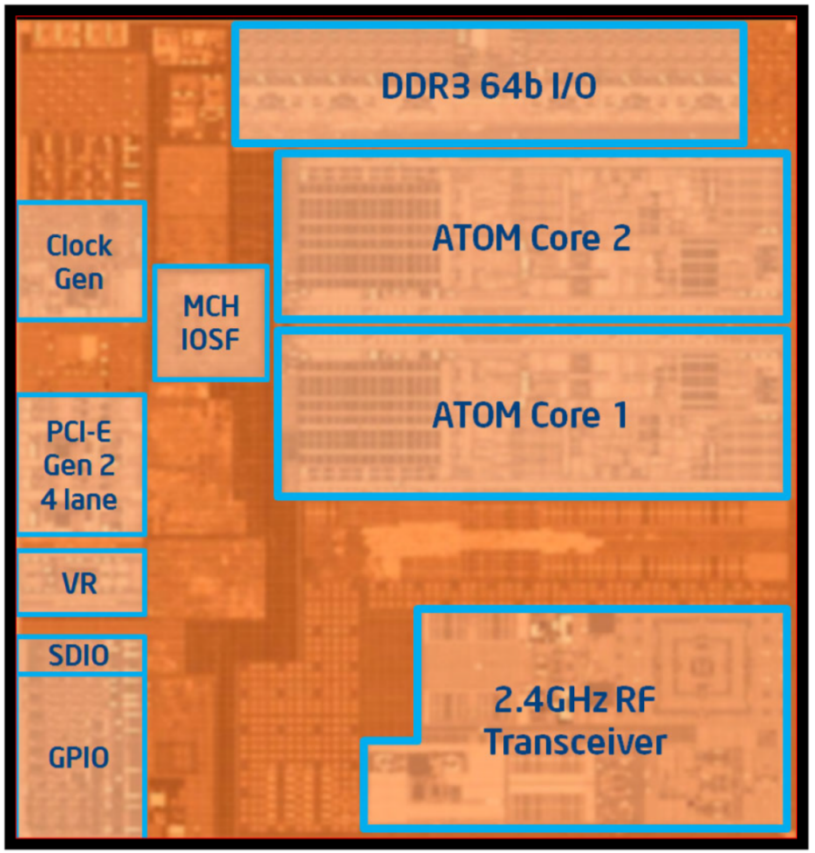
[2]Intel, Hillsboro, OR

Outline

- **Introduction**
- **Proposed Architecture**
- **Open Loop Fractional Divider**
- **Circuit Implementation**
- **Measurement Results**
- **Conclusions**

SoC Clocking

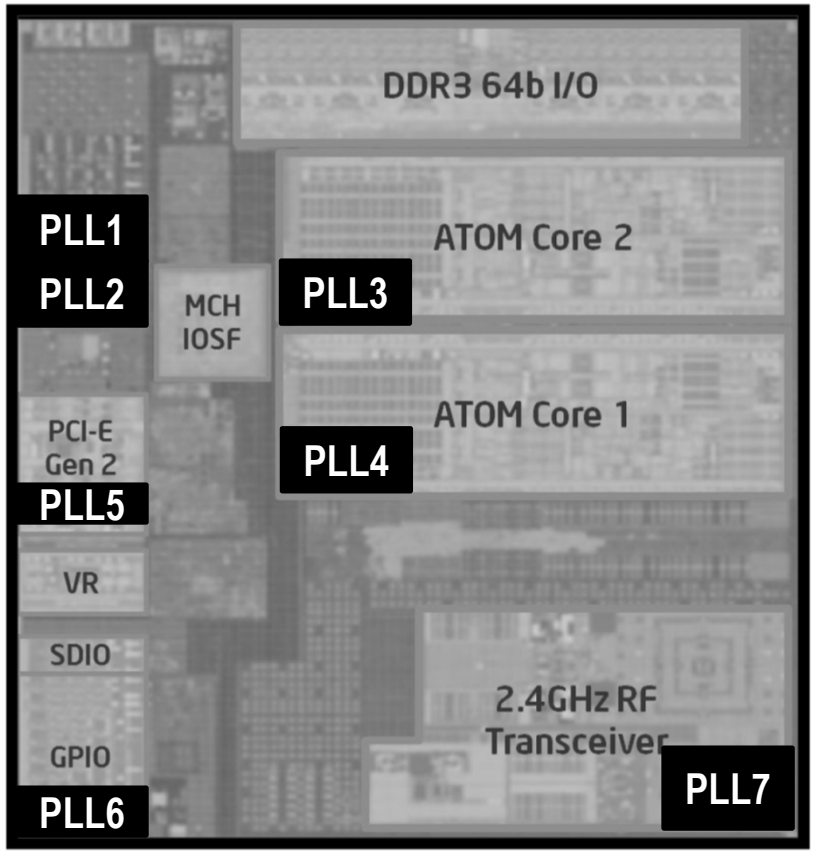
- Modern SoC modules:
  - Multicore processors
  - Memories
  - I/O interfaces
  - Power management
  - Wireless transceivers
- Multiple clock domains with different requirements



[Lakdawala, ISSCC 2012]

SoC Clocking Challenges

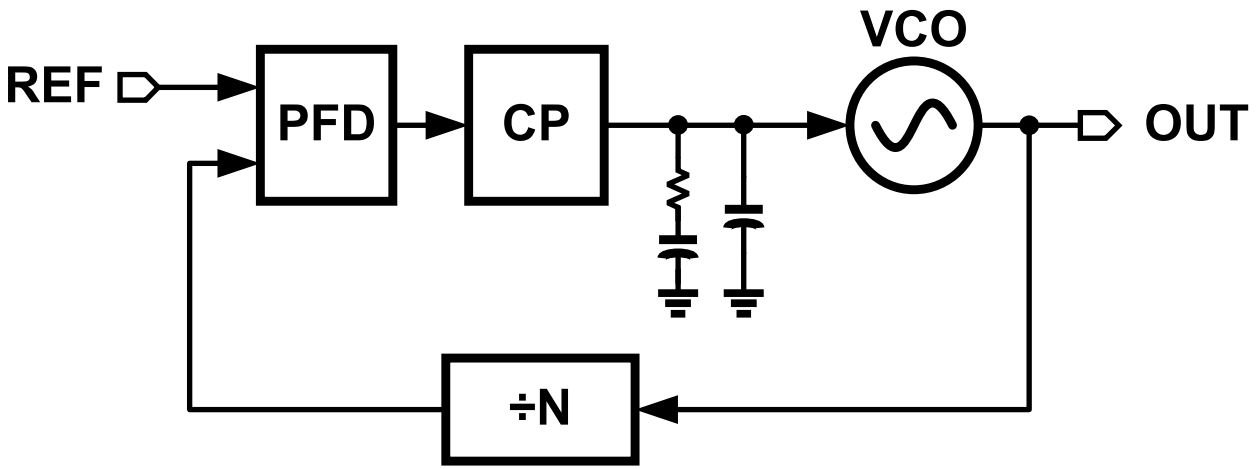
- Multiple blocks w/ different PLLs
- Requirements include:
  - Wide frequency range
  - Fine frequency resolution
  - Spread Spectrum Clocking (SSC)
  - Fast frequency switching for DFS
  - Low jitter/Low power/Small area



Motivation: Generic clock generator satisfying these requirements

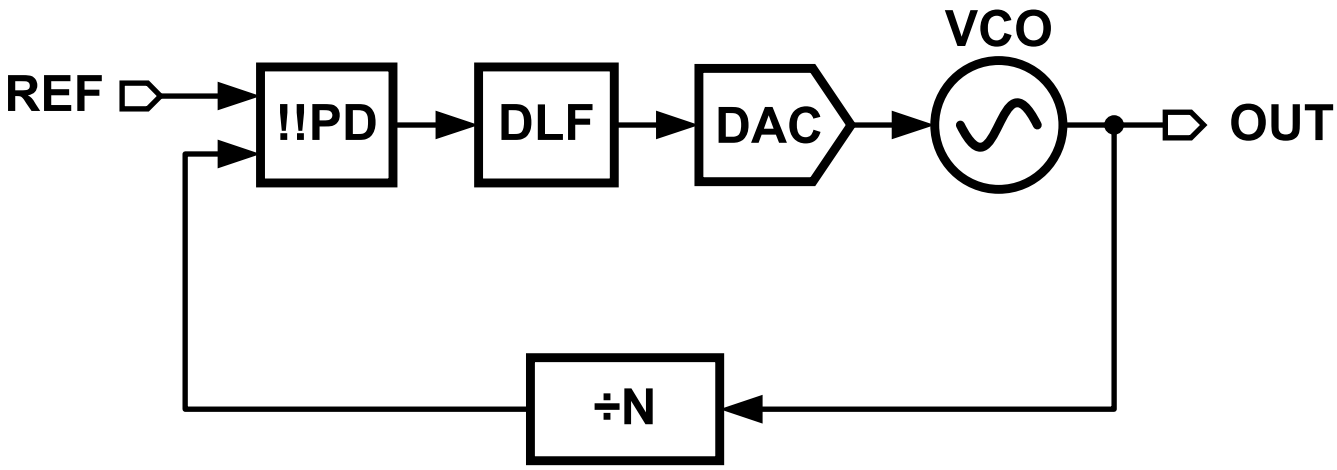
[Lakdawala, ISSCC 2012]

Prior Art: Analog Integer-N PLL



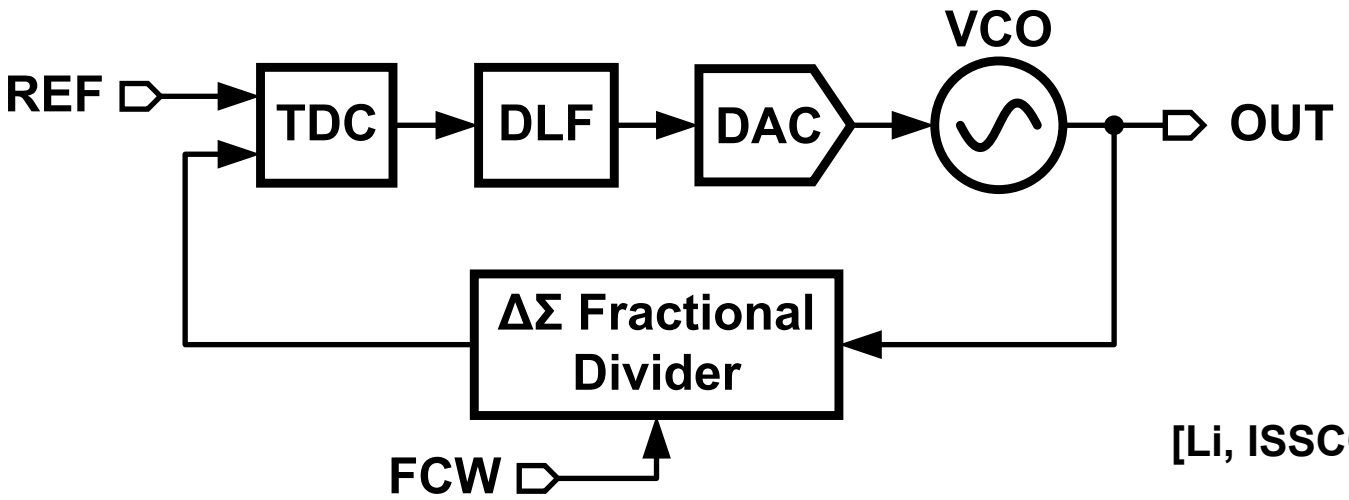
- ✓ **Low Jitter**
- × **Inflexible, not scalable, large area**
- × **Resolution is limited by reference**
- × **Not capable of SSC or DFS**

Prior Art: Digital Integer-N PLL



- ✓ Low Jitter
- ✓ All-digital: reconfigurable, scalable, small area
- × Resolution is limited by reference
- × Not capable of SSC or DFS

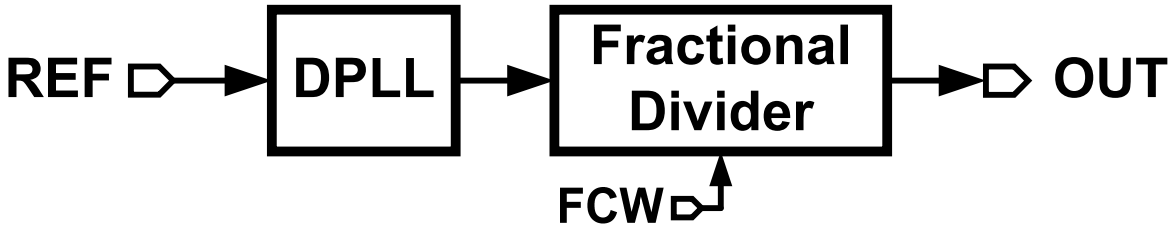
Prior Art: Digital Fractional-N PLL

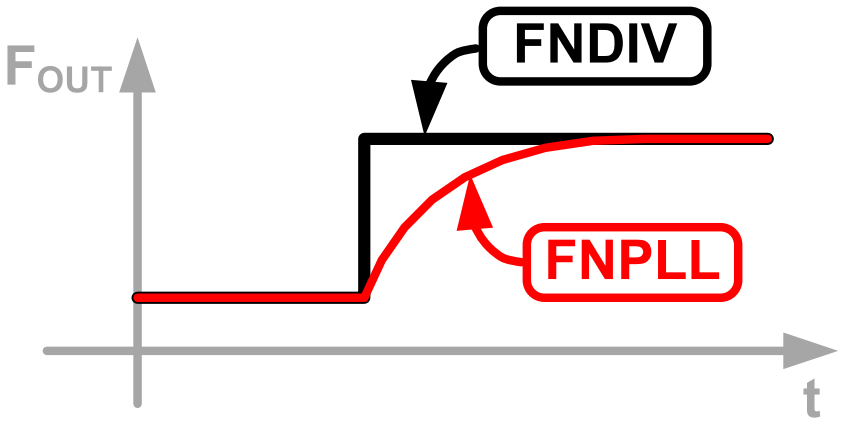


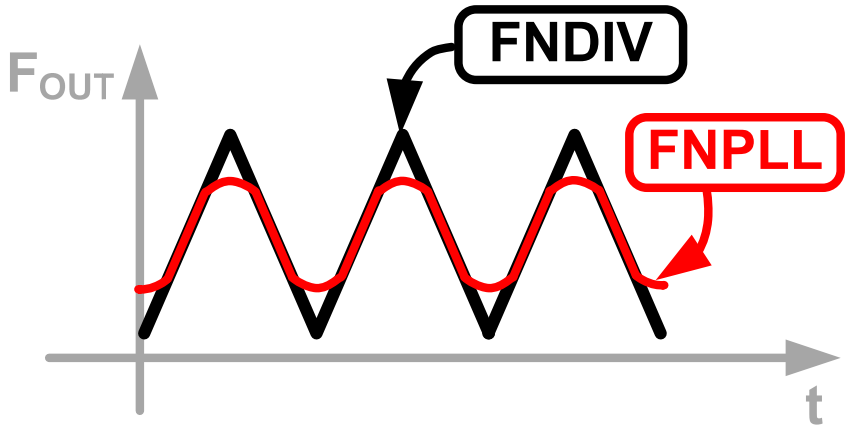
[Li, ISSCC 2012]

- ✓ All-digital: reconfigurable, scalable, small area
- ✓ Fine frequency resolution, SSC and DFS capability
- × Narrow BW limits SSC and frequency switching
- × Noise BW tradeoff TDC vs DCO, high power or jitter

Open-Loop Fractional Divider





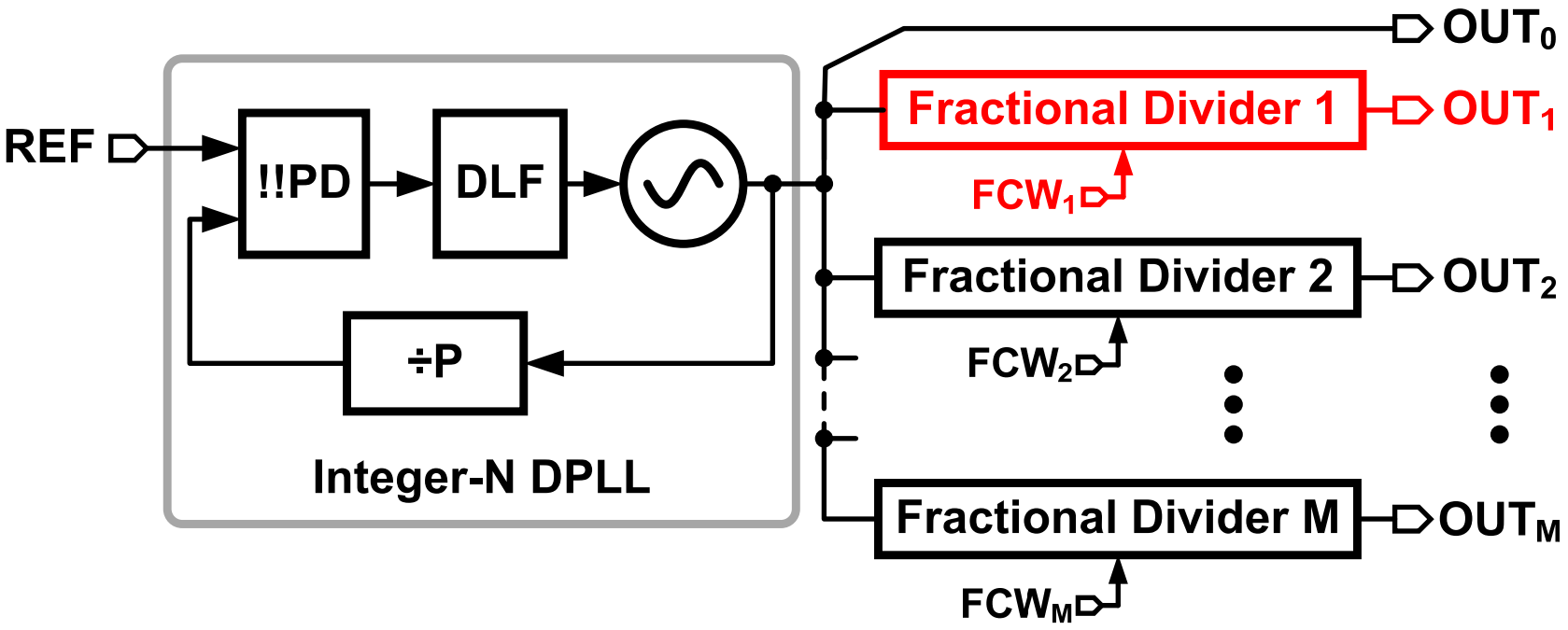


Instantaneous frequency switching

SSC with no filtering → Large EMI reduction

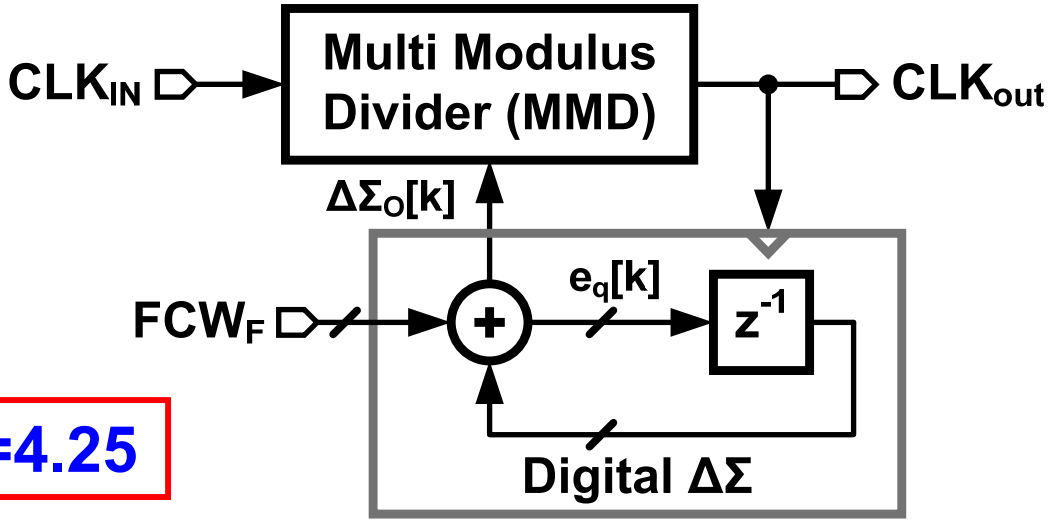
Proposed Architecture

Integer-N DPLL + Open-loop fractional divider

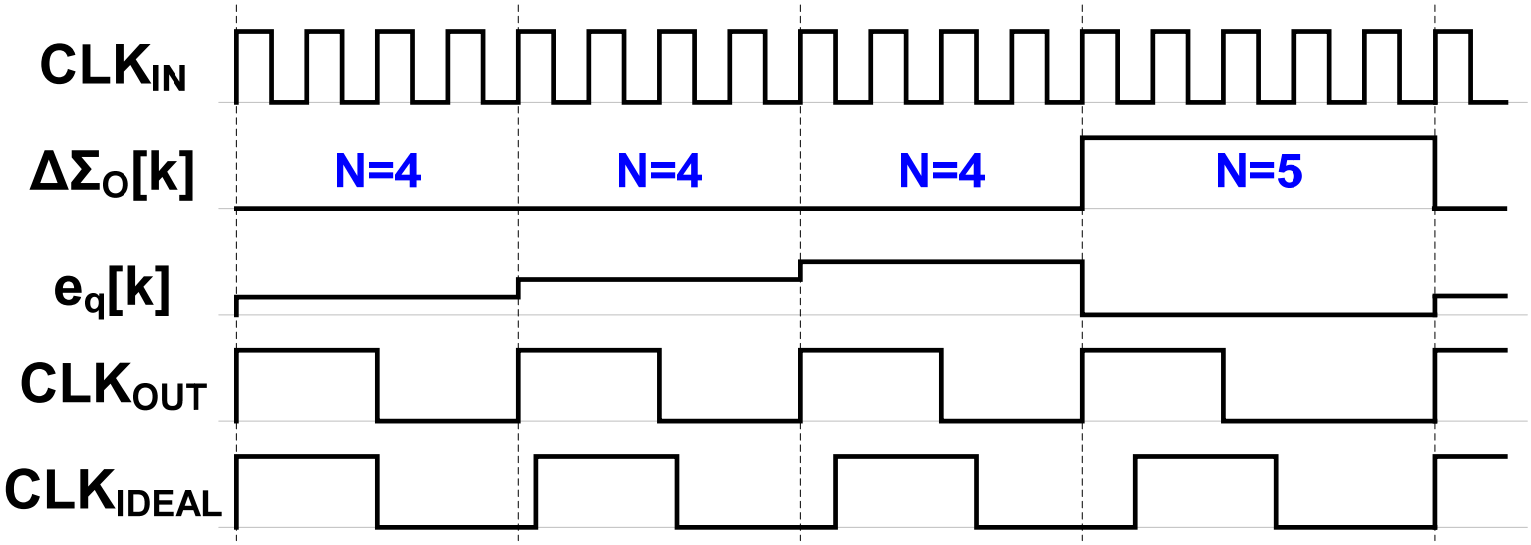


- **Fractional-N frequency synthesis:** $F_{OUT} = \frac{P}{N+\alpha} \times F_{REF}$

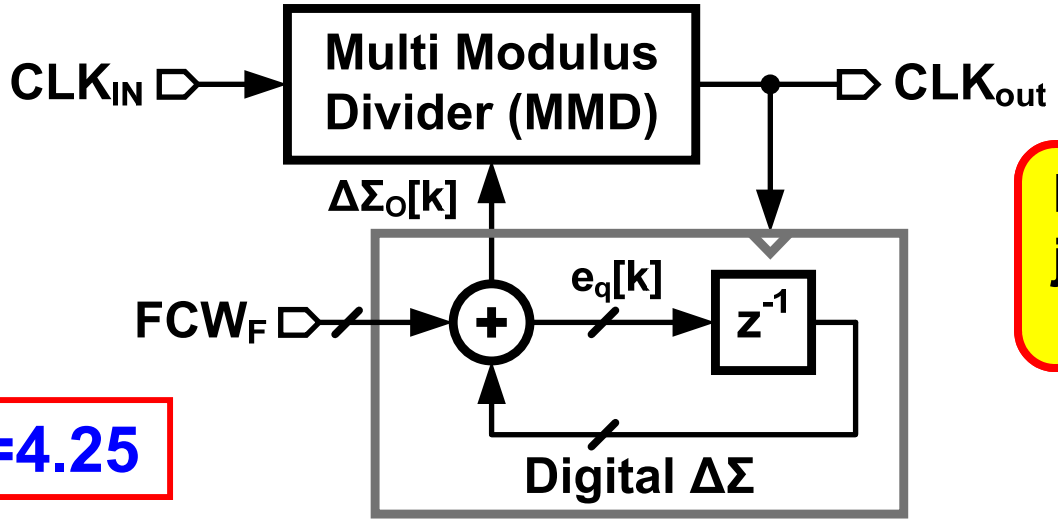
ΔΣ Fractional Divider



FCW=4.25



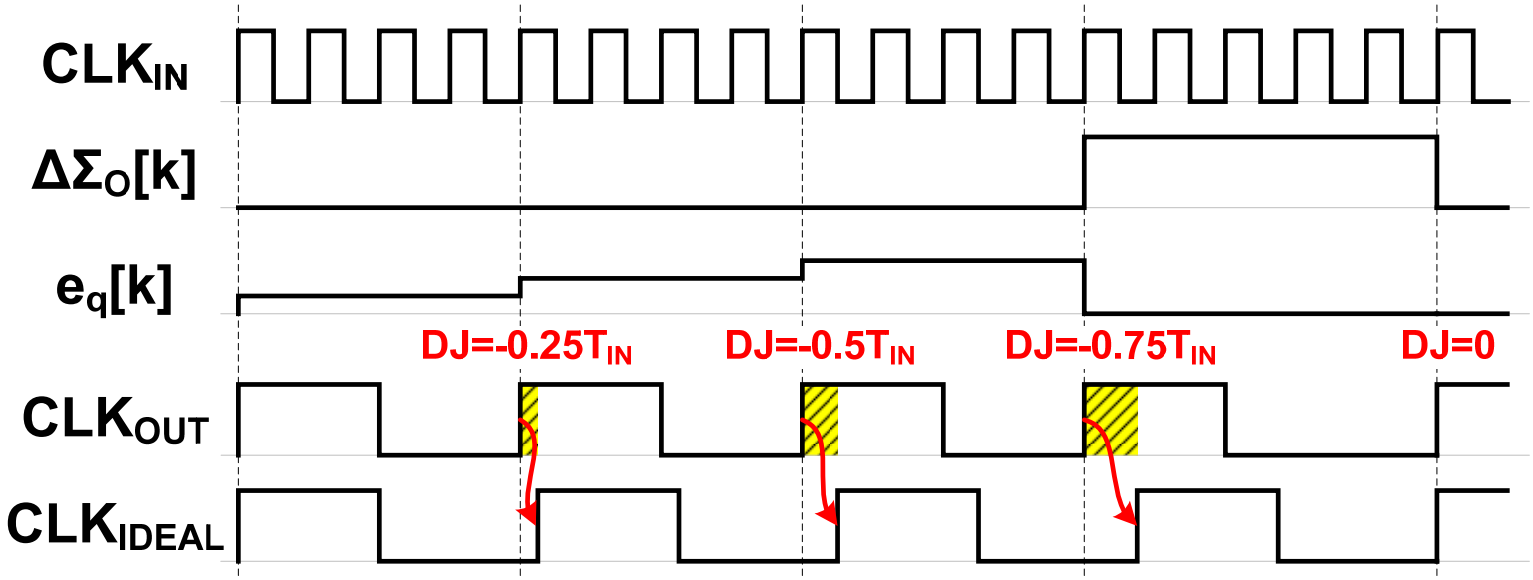
ΔΣ Fractional Divider



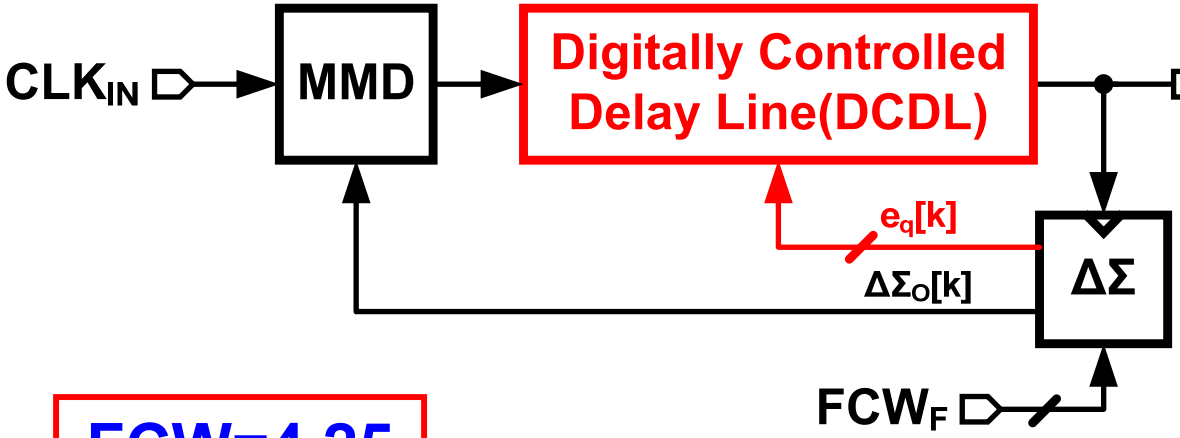
Large deterministic jitter (DJ) due to ΔΣ truncation error

FCW=4.25

$$DJ = -e_q \times T_{IN}$$



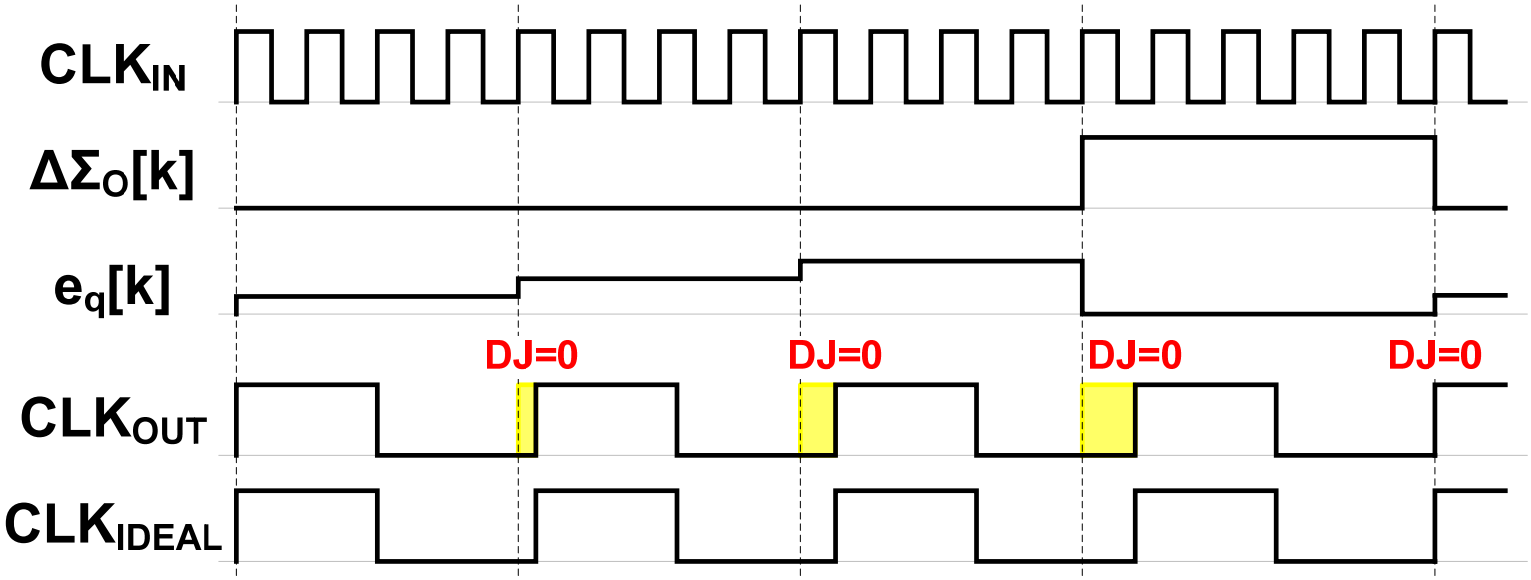
Open-Loop ΔΣ Fractional Divider



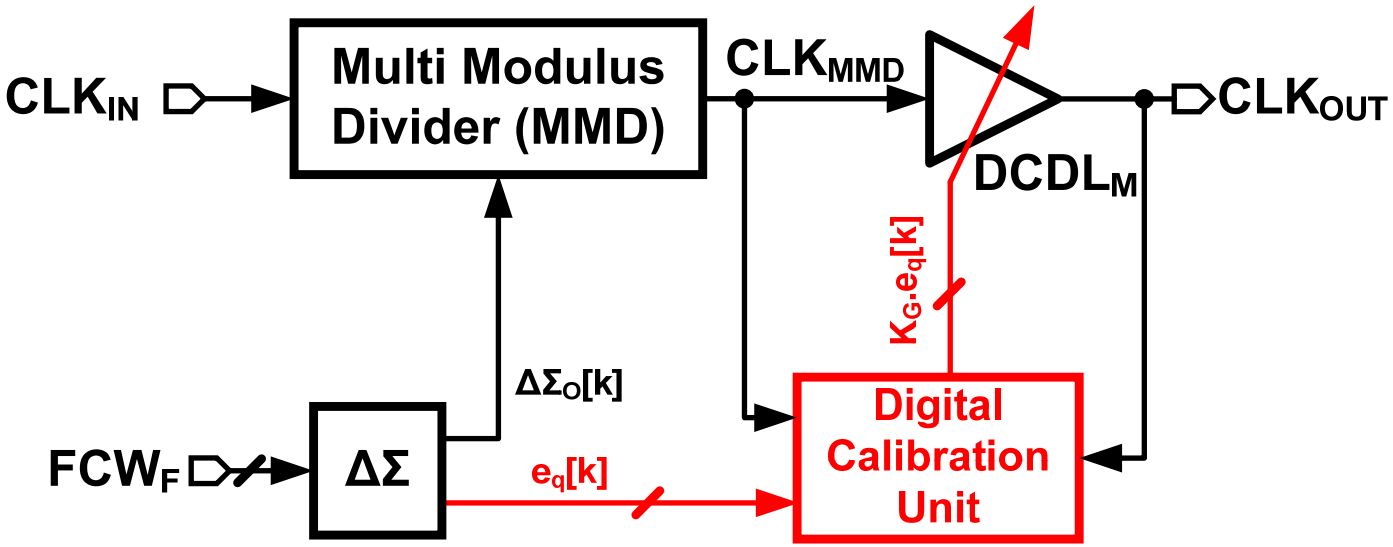
ΔΣ Quantization Noise Cancellation (QNC) using DCDL

FCW=4.25

$$T_{QNC} = e_q \times T_{IN}$$



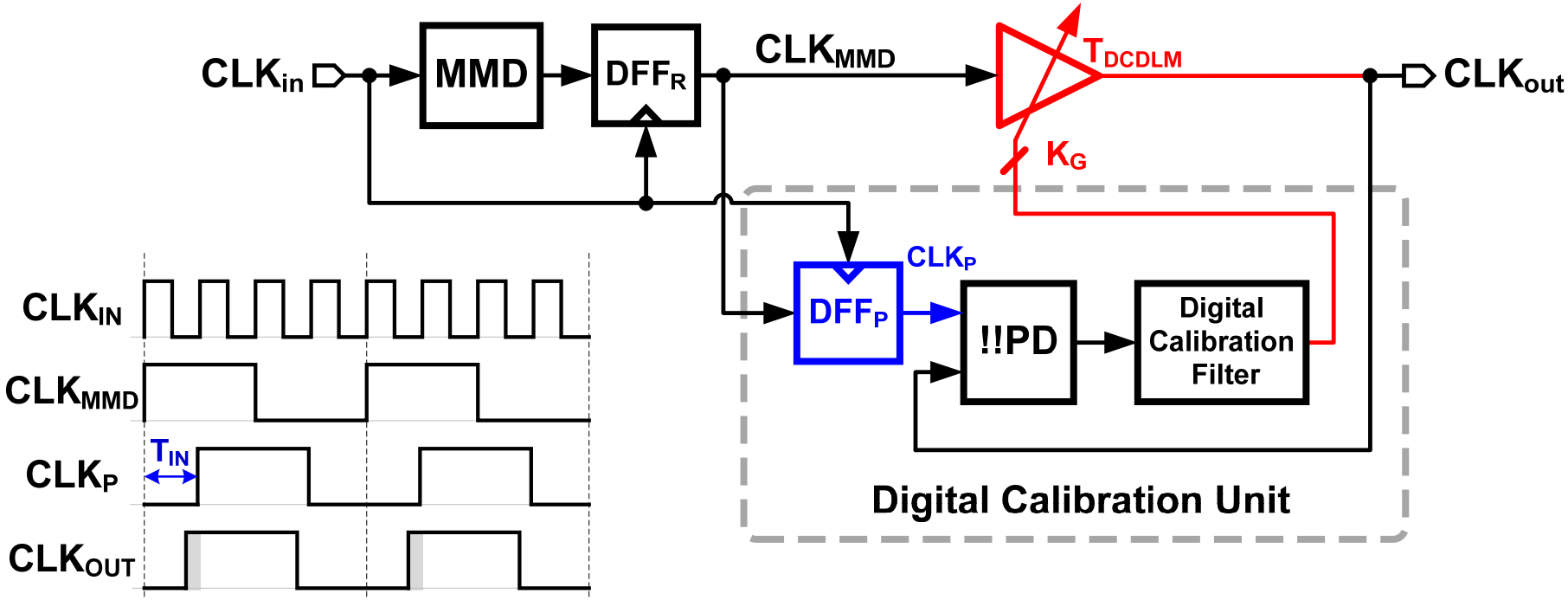
Proposed DCDL Gain Calibration



- DCDL gain is calibrated to be T_{IN} by digitally scaling $e_q[k]$ by a factor K_G

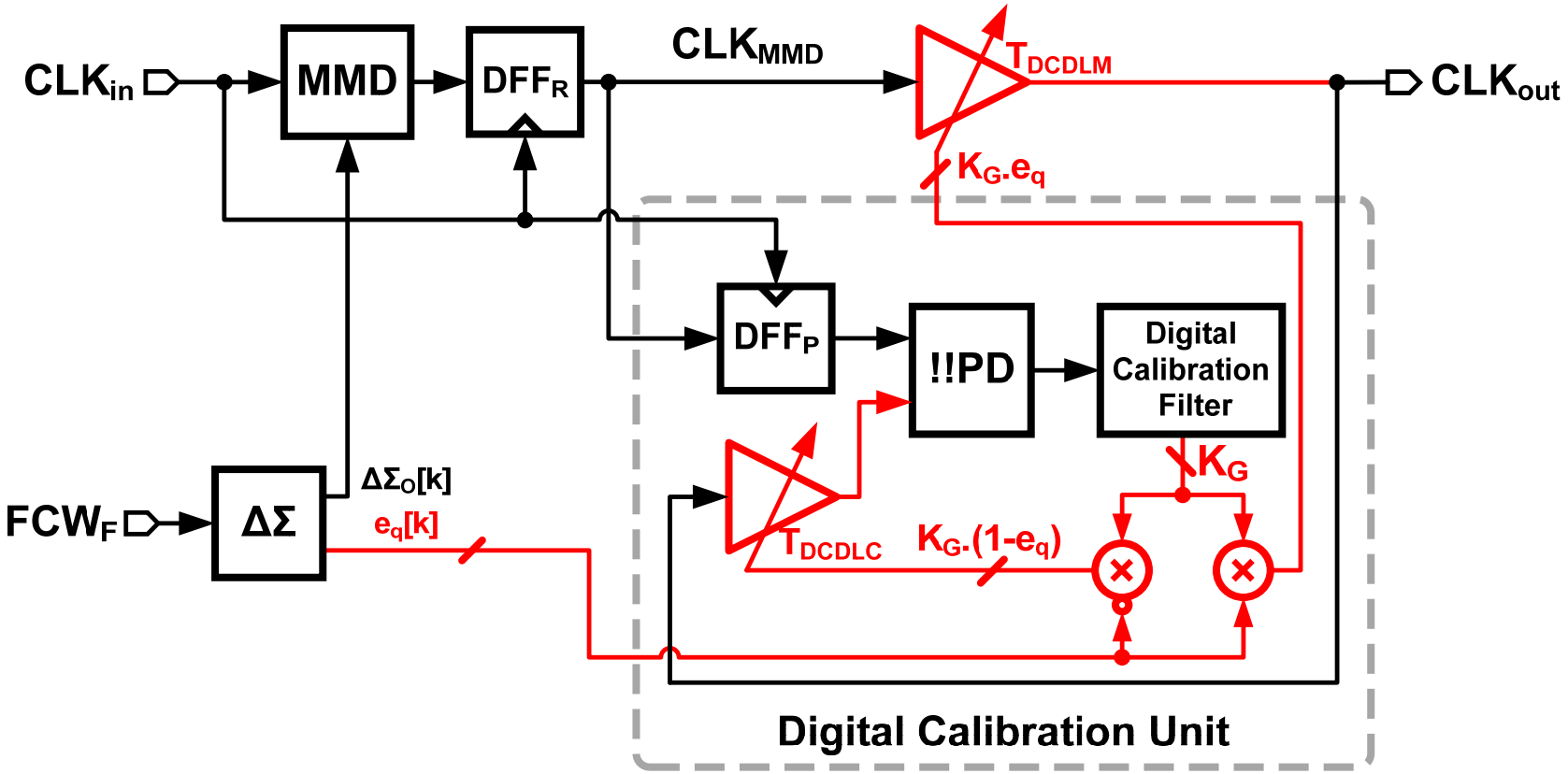
$$K_G \times T_{DCDLM} = T_{IN}$$

DCDL Gain Calibration: Foreground



- Generate T_{IN} time reference using matched DFF
- Lock DCDL delay to T_{IN} using DLL
- Sensitive to supply and temperature variations

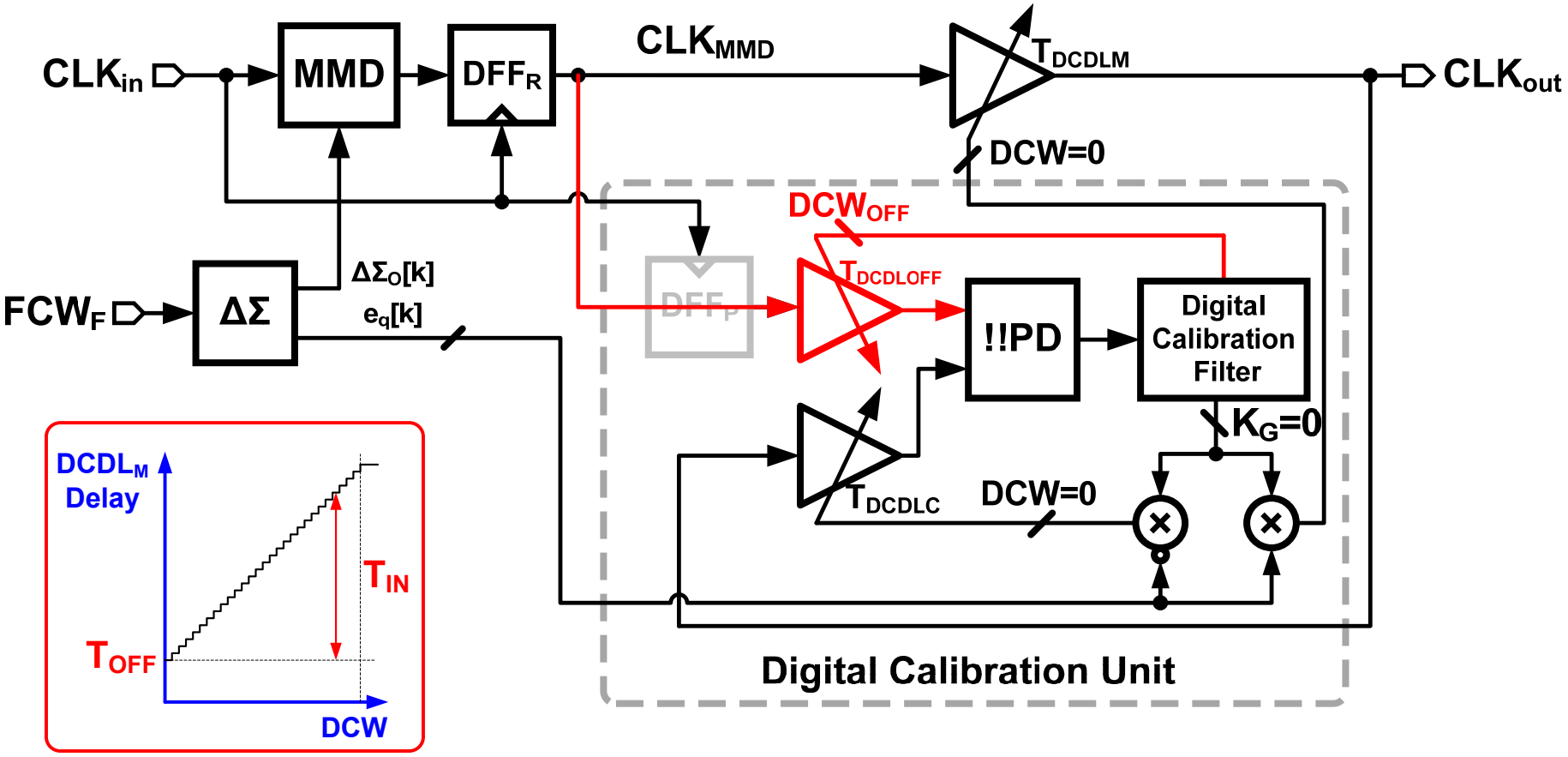
DCDL Gain Calibration: Background



- **Background Calibration using a complementary DCDL**

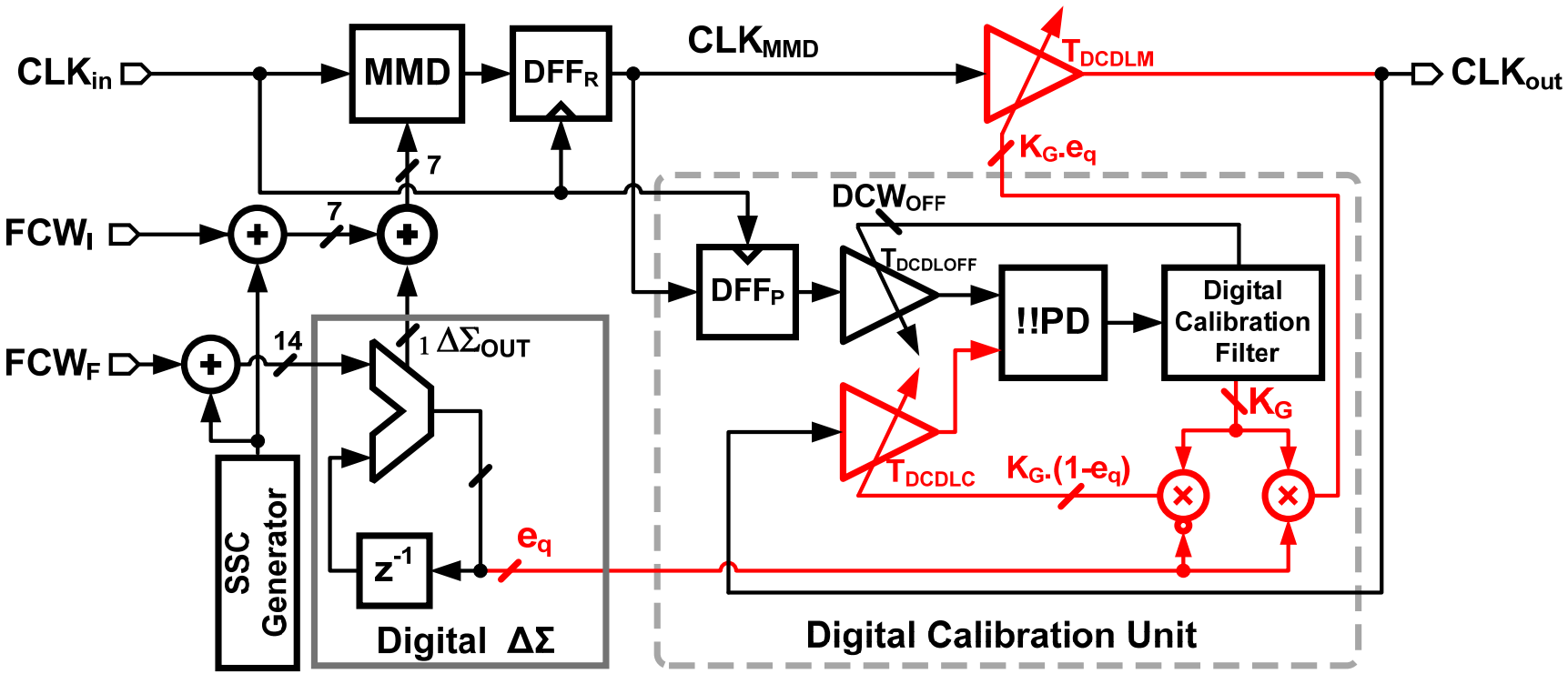
$$e_q K_G T_{DCDLM} + (1 - e_q) K_G T_{DCDLC} = T_{IN} \quad \Rightarrow \quad K_G \times T_{DCDLM} = T_{IN}$$

DCDL Offset Cancellation



- DCDL has non-zero delay (T_{OFF}) for zero input code
- $DCDL_{OFF}$ is added to cancel this offset

Complete Fractional Divider



- ☺ Wide frequency range
- ☺ Low jitter, low power
- ☺ Programmable SSC
- ☺ Fine frequency resolution
- ☺ Insensitive to PVT variations
- ☺ Inst. frequency switching

Outline

- Introduction
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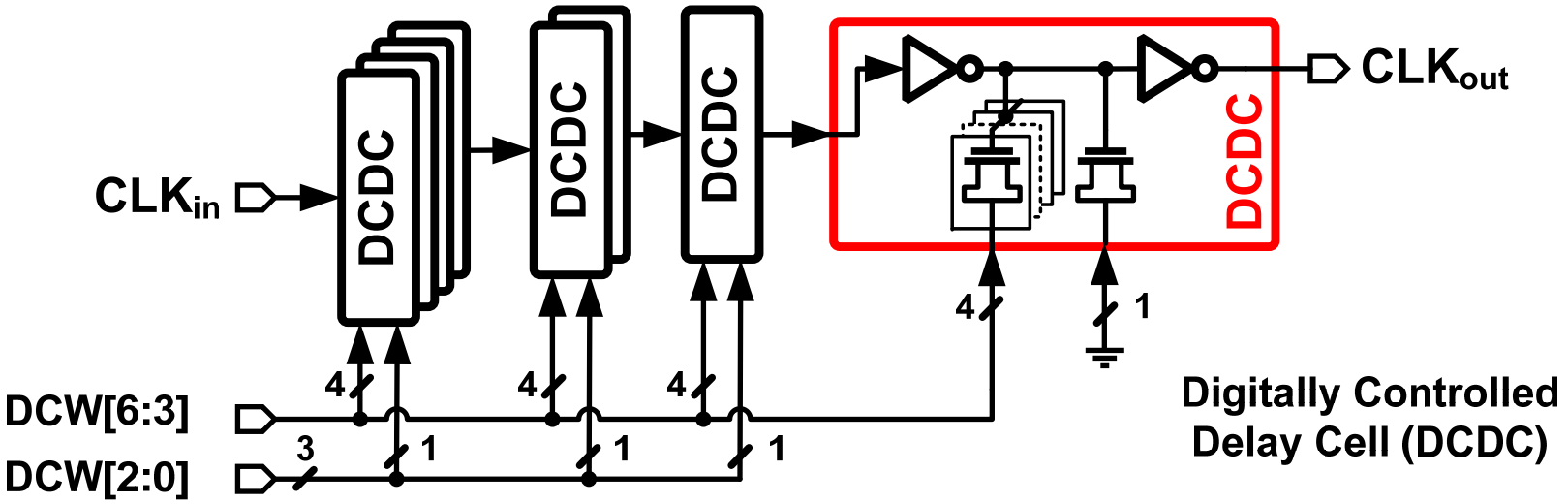
- **Circuit Implementation**
- Measurement Results
- Conclusions

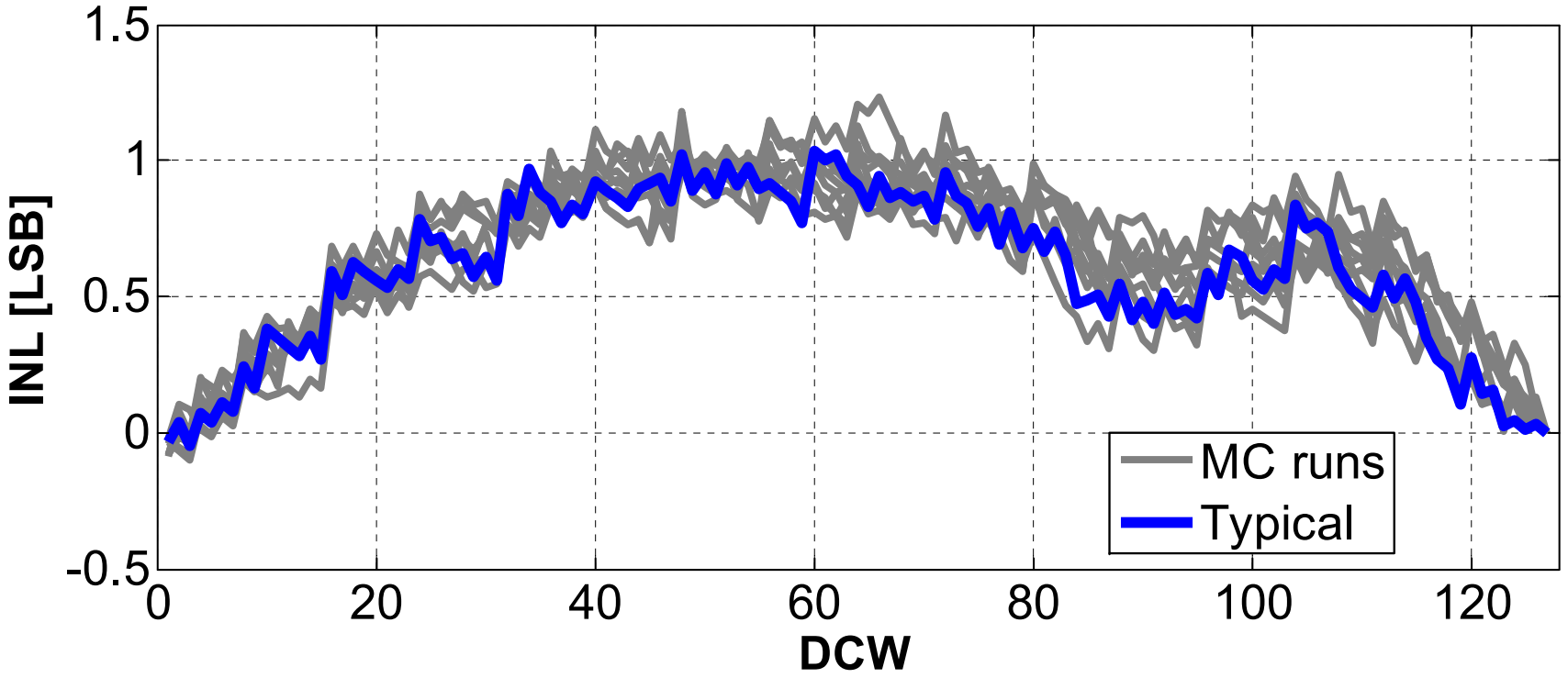
DCDL Implementation



- **Fast rise/fall times to reduce DCDL sensitivity to:**
  - **Supply/thermal noise**
  - **Mismatch**
- **Segmented control to improve DCDL linearity**

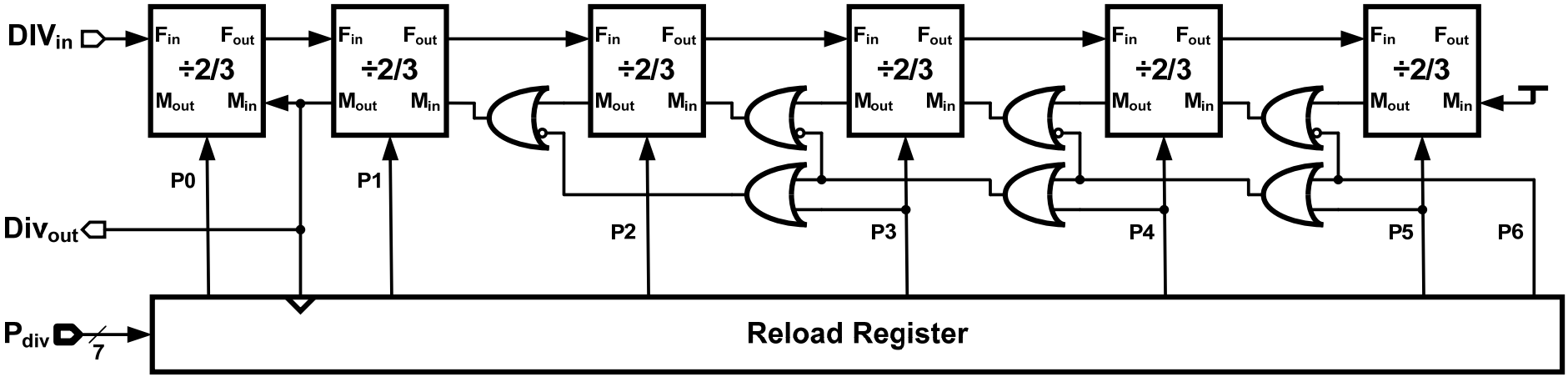
DCDL Simulation

- 7b DCDL , LSB resolution ~ 2ps
- Post-layout simulations shows INL < 1.25LSB.



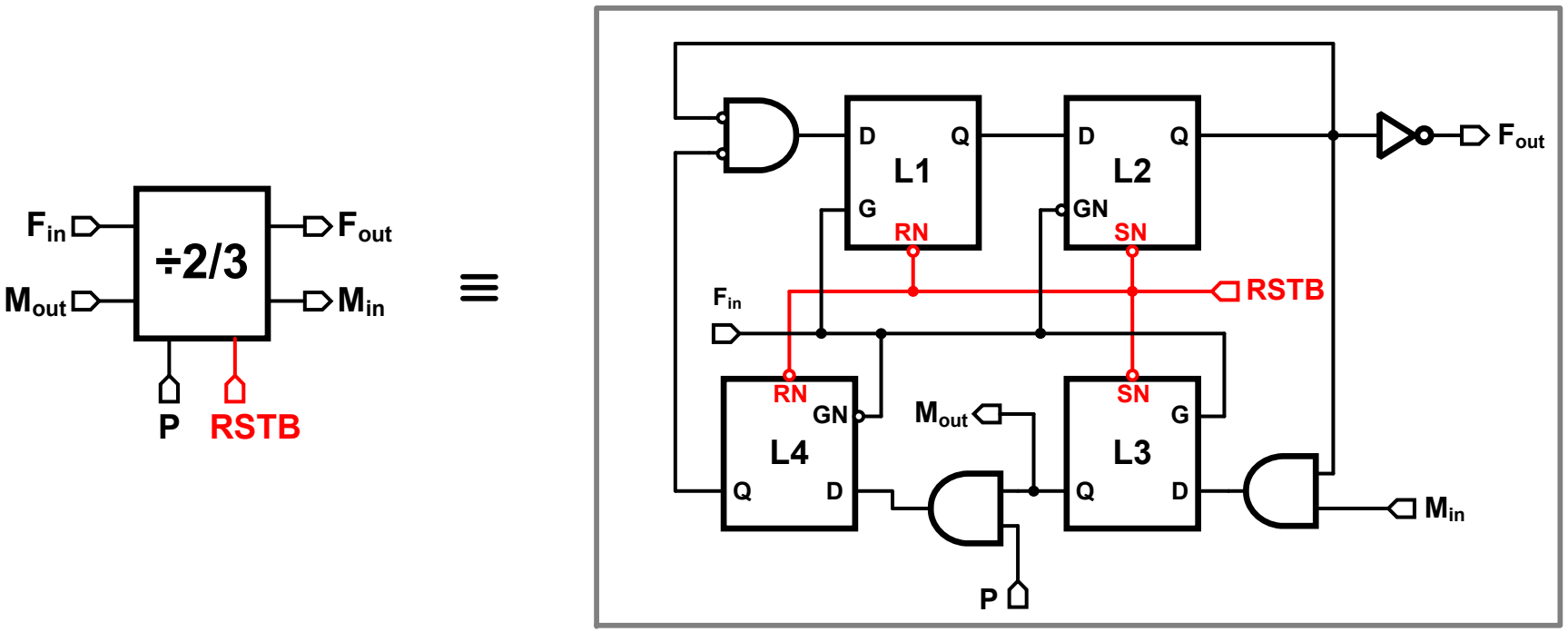
Conventional Extended Range MMD

[Vaucher, JSSC 2000]



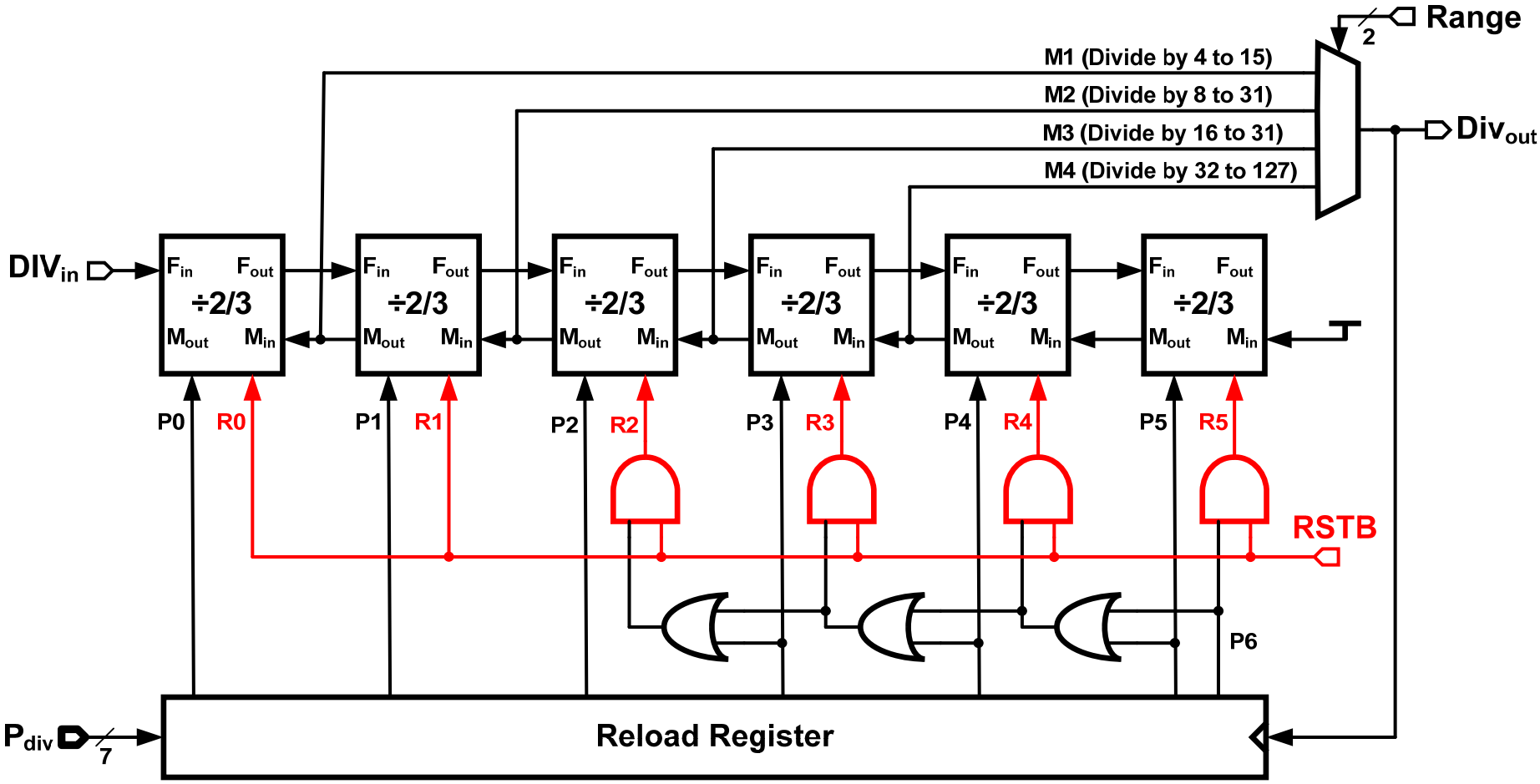
- MMD with n-stages has limited range: $2^n \rightarrow 2^{n+1}-1$
- Range can be extended by deactivating last stages
- Fractional operation fails at extension boundaries

Divide-by-2/3 with Reset



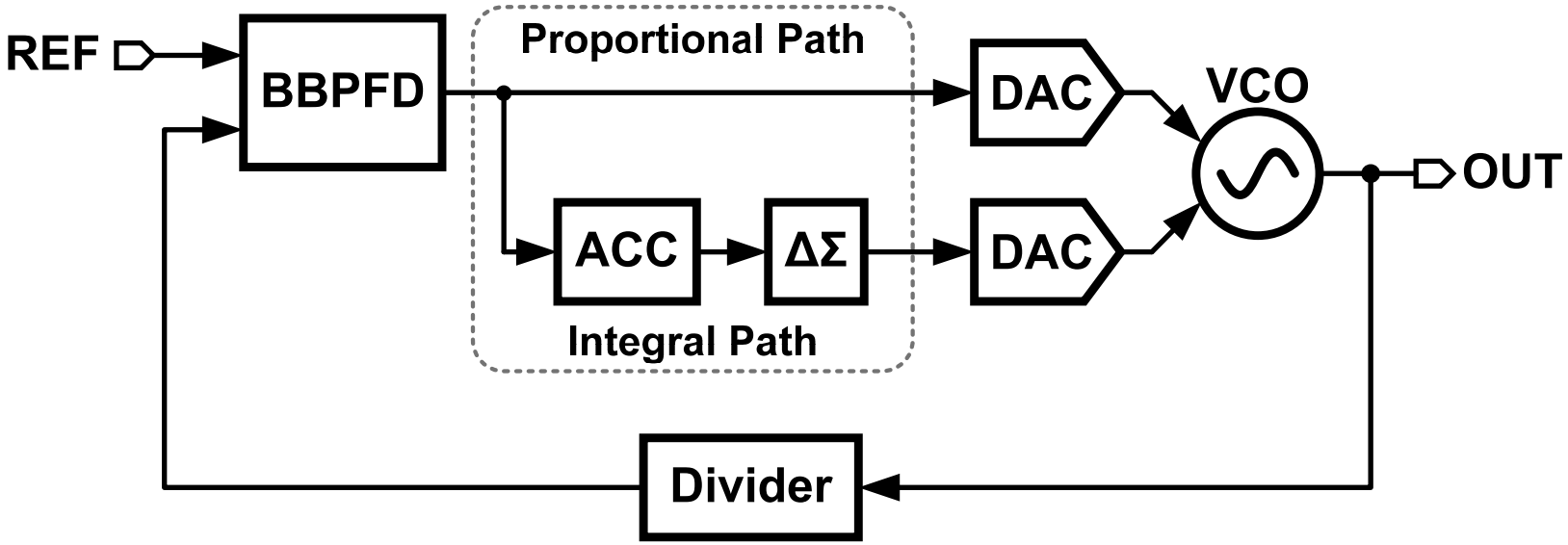
- **Reset ensures seamless switching at extension boundaries**

Proposed Extended Range MMD



- **Wide division range 4→127 with seamless switching**

Integer-N DPLL



- Simple, scalable implementation
- Reduced analog complexity
- 100MHz reference, 5GHz output

Outline

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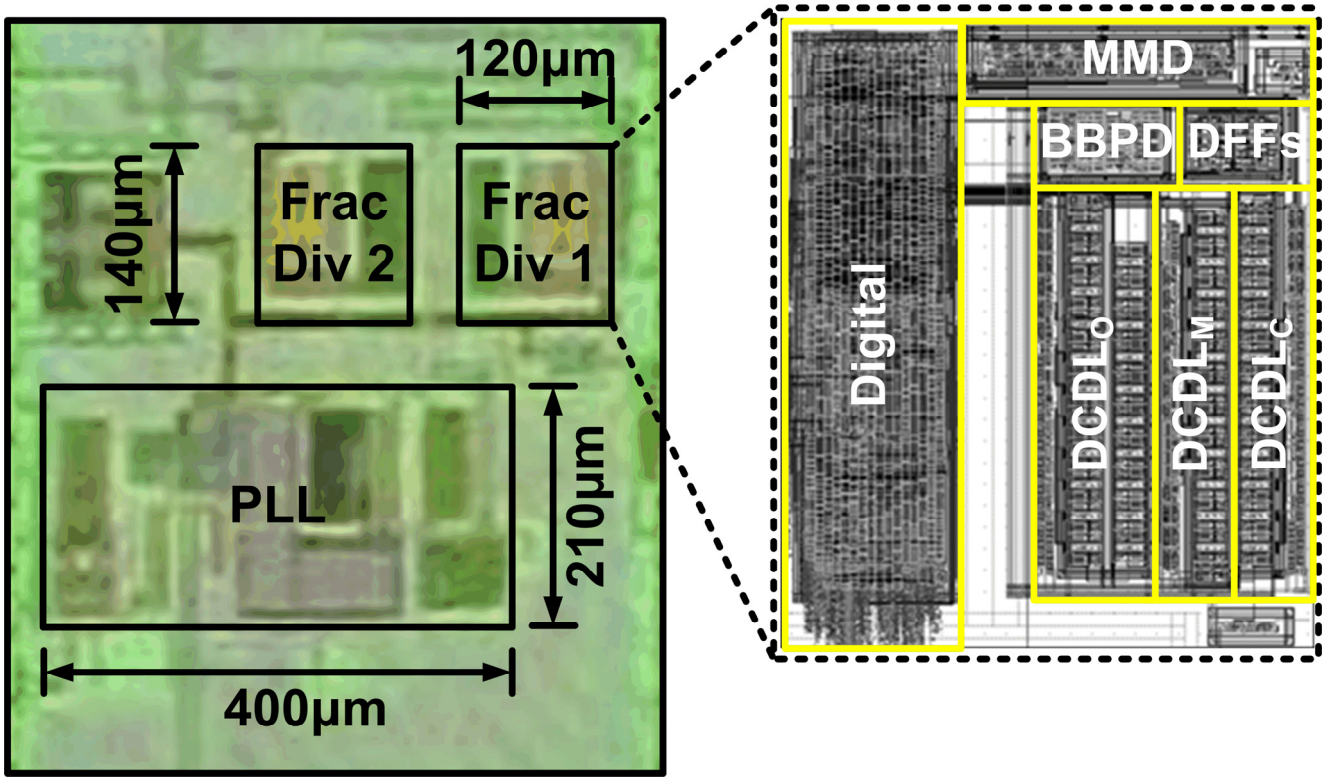
- Conclusions

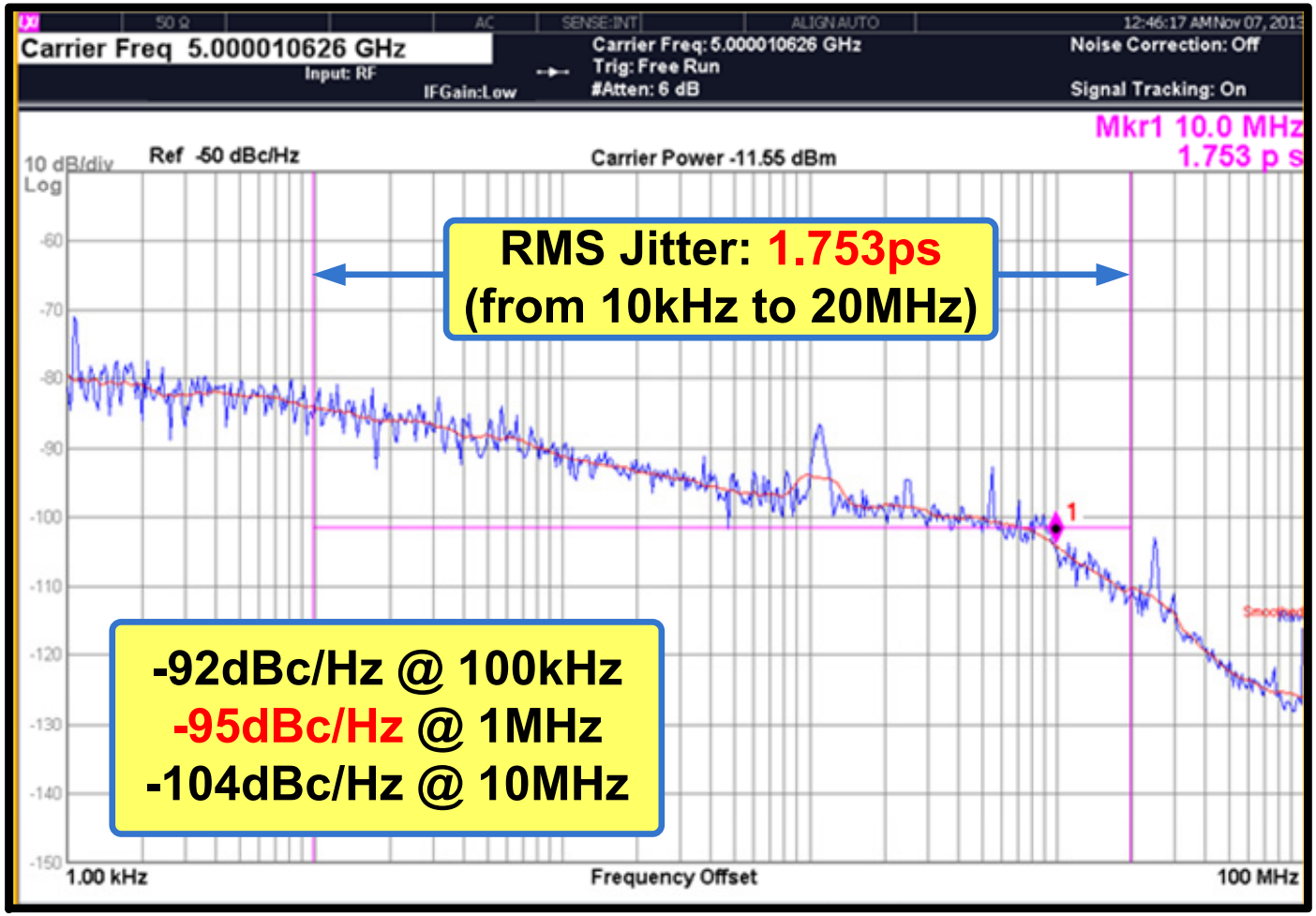
Die Photograph

- 65nm CMOS
- Active area: 0.12mm^2 (fractional divider ~ 0.017mm^2)
- VDD: 0.9V



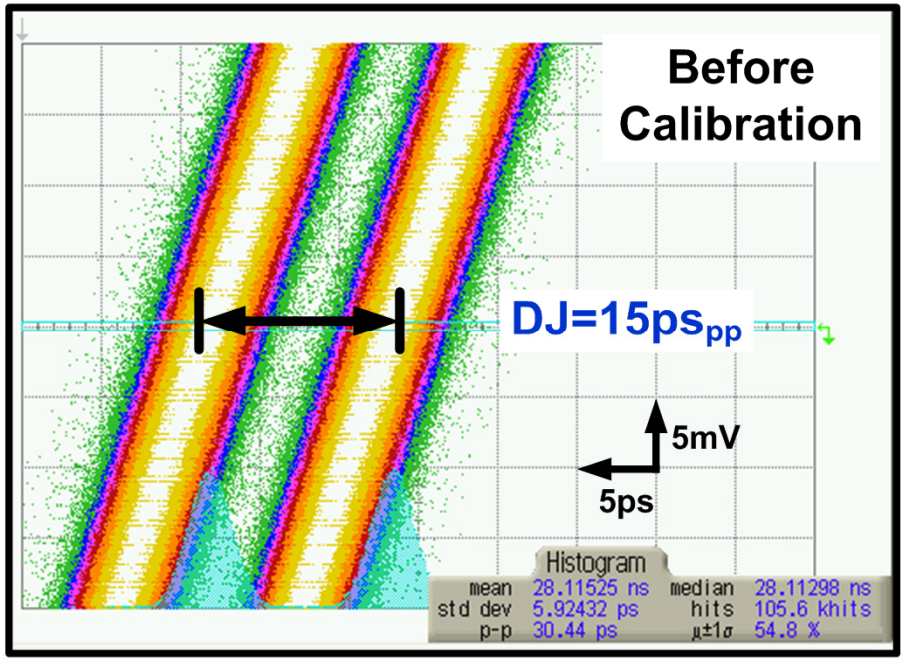
DPLL Phase Noise at 5GHz

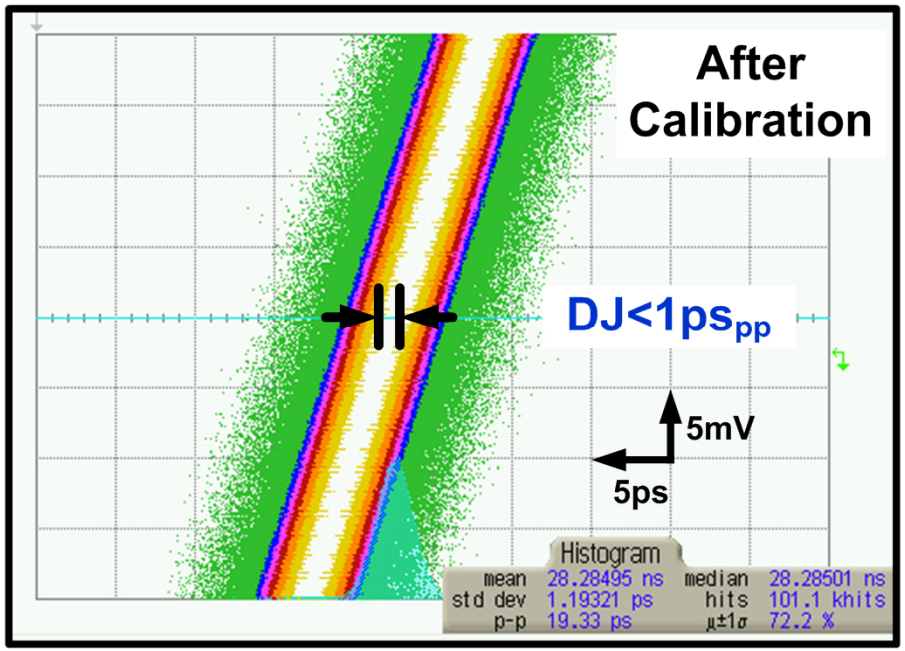
- Low Jitter ~ 1.75ps$_{rms}$, Low Power < 4mW



Fractional Divider Jitter at 975MHz

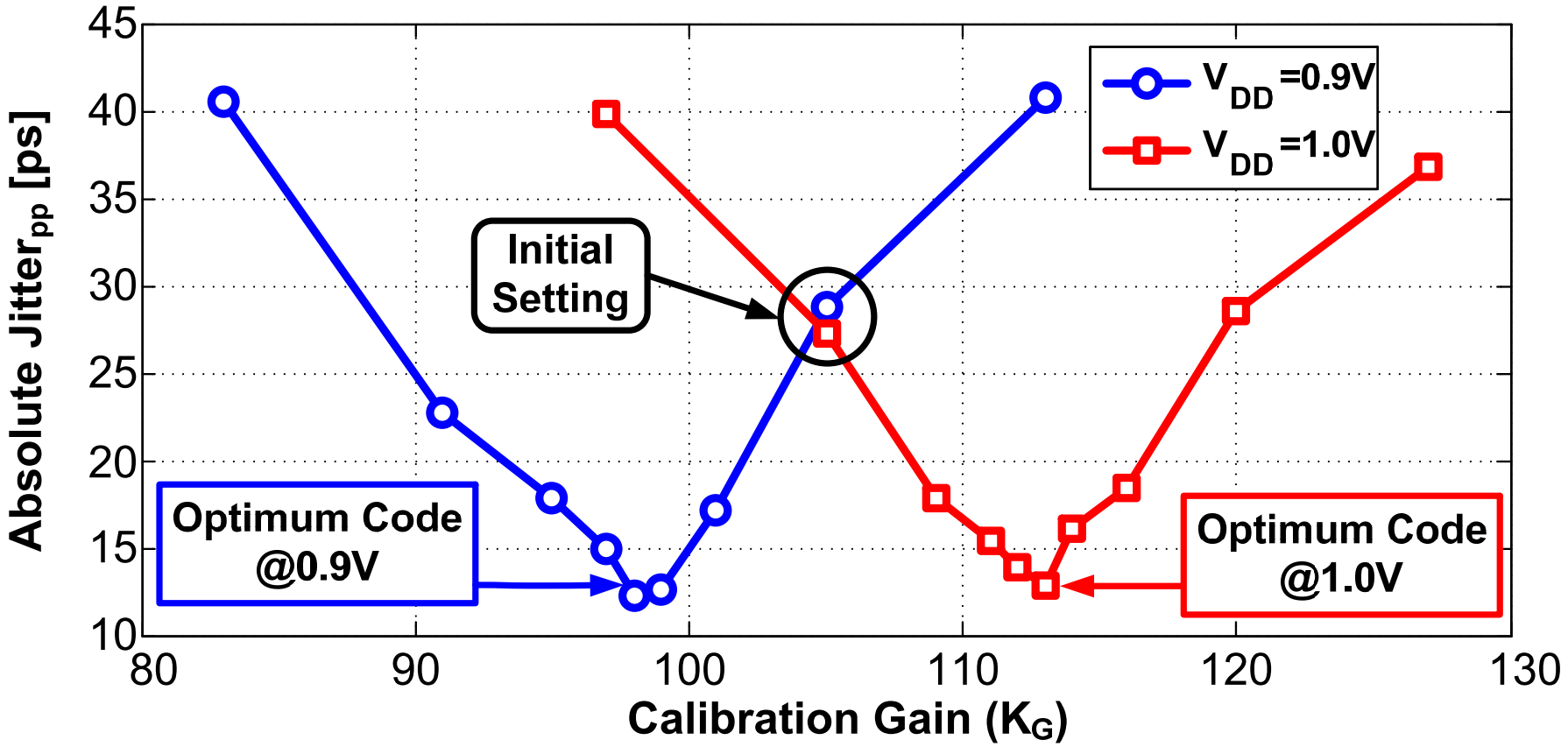
- Before calibration: ΔΣ noise is not perfectly canceled
- After calibration: DJ reduced to 1ps





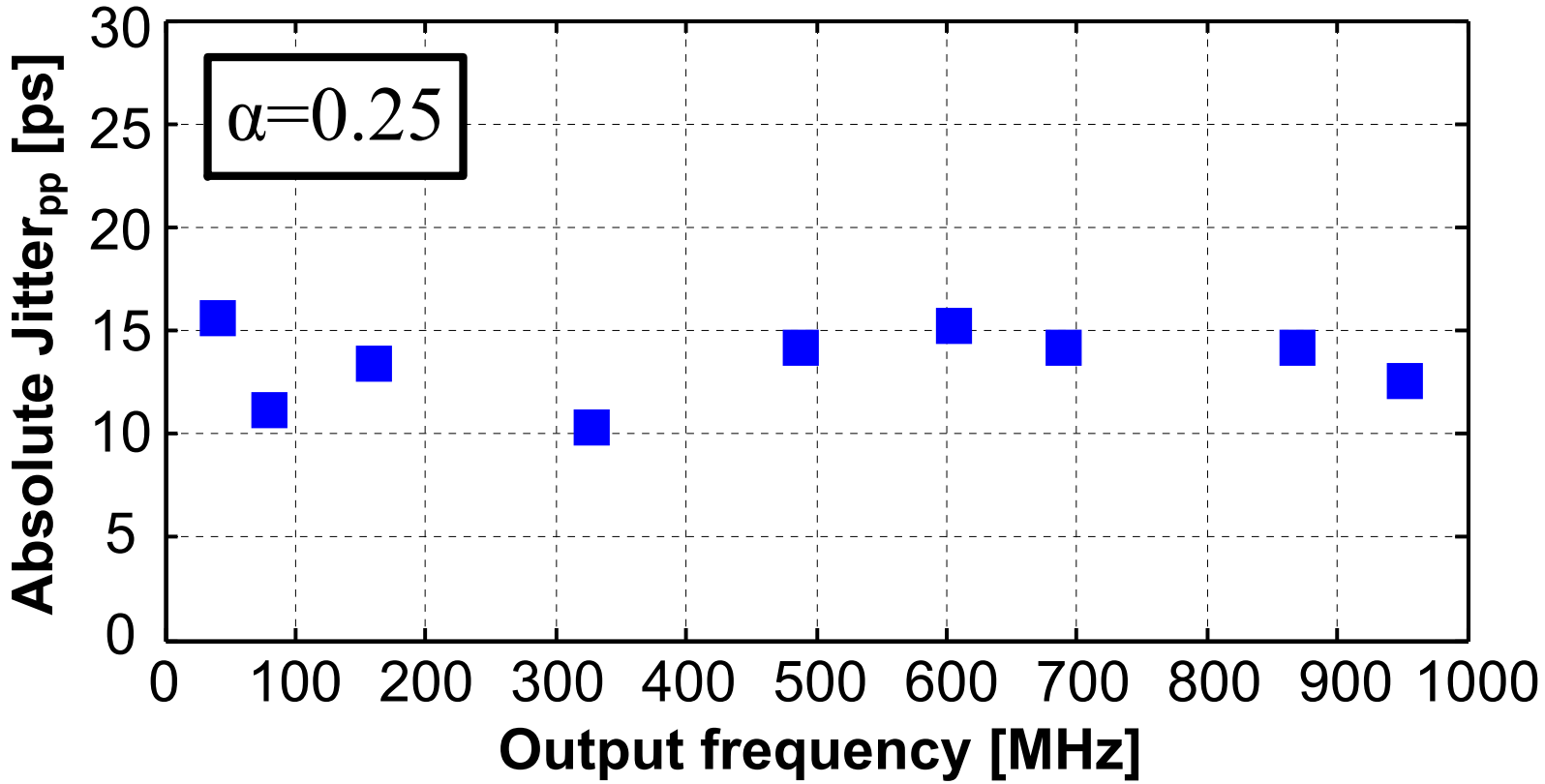
Jitter Vs Calibration Gain (K_G)

- Optimum calibration code shifts with supply voltage
- Loop always settle to optimum code



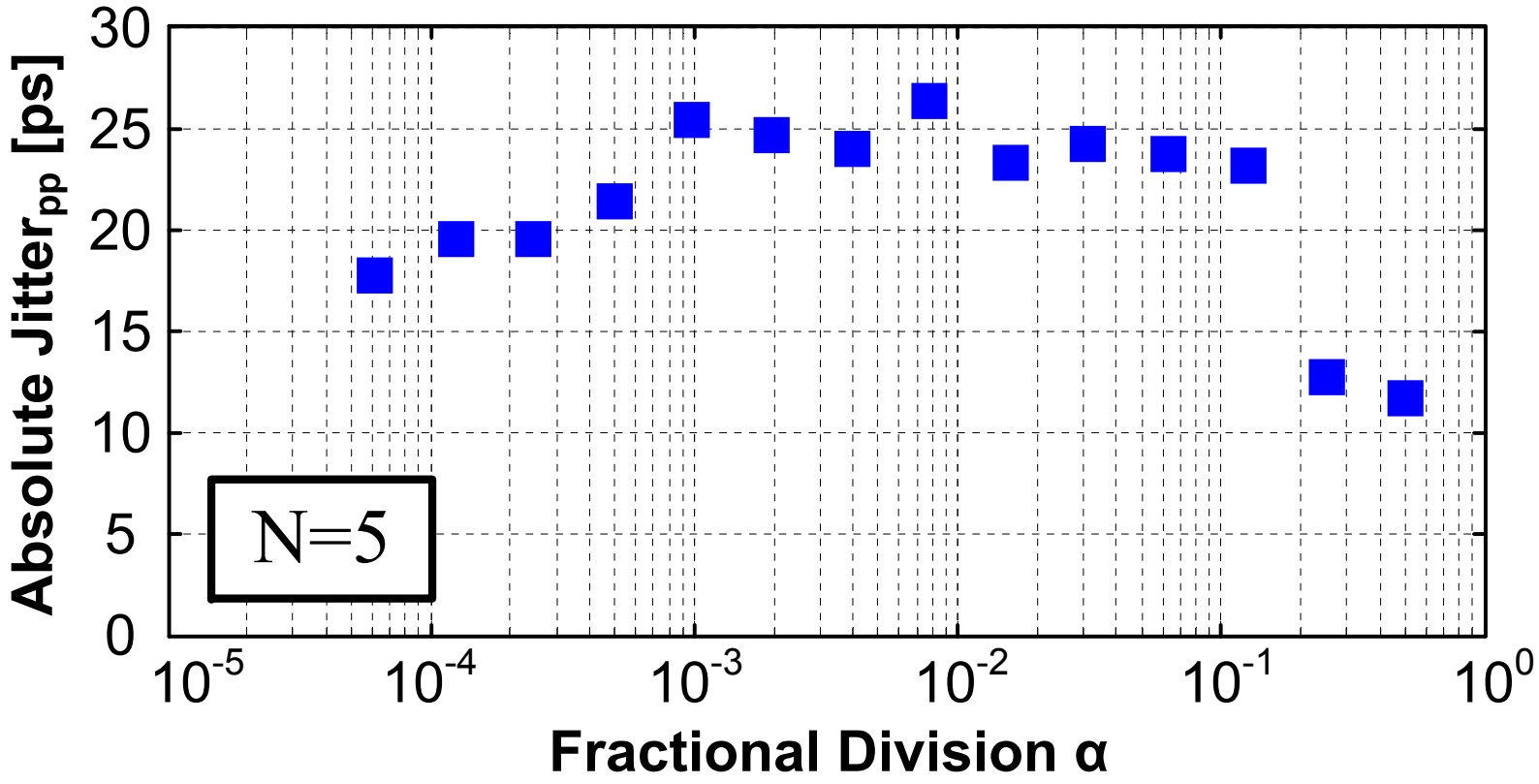
Jitter Vs Output Frequency

- Wide frequency range (20MHz-1000MHz)
- Jitter < 20ps$_{pp}$ over the entire range



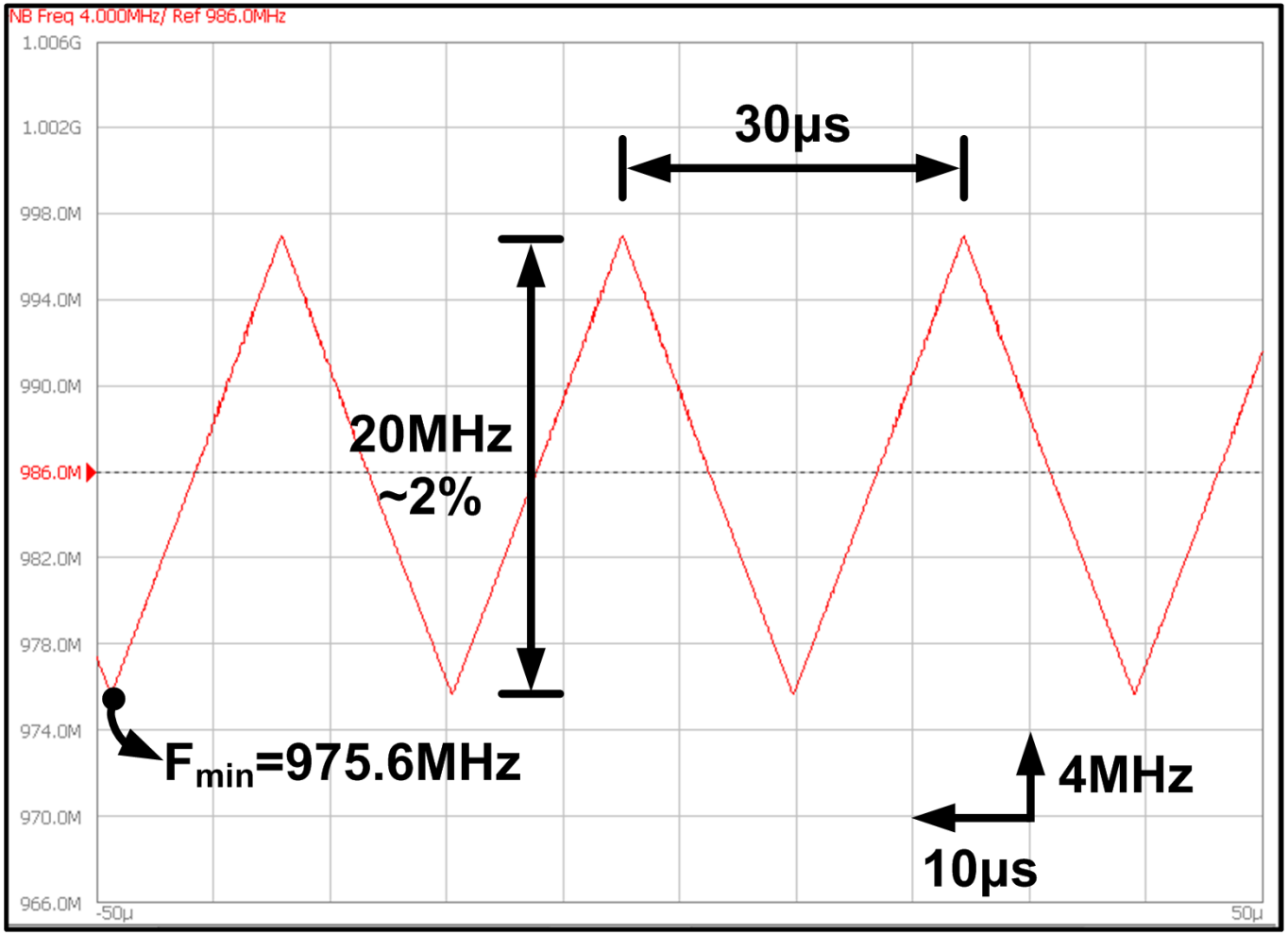
Jitter Vs Fractional Division Ratio

- 14-bit fractional resolution
- Jitter increased to 27ps$_{pp}$ due to DCDL non-linearity



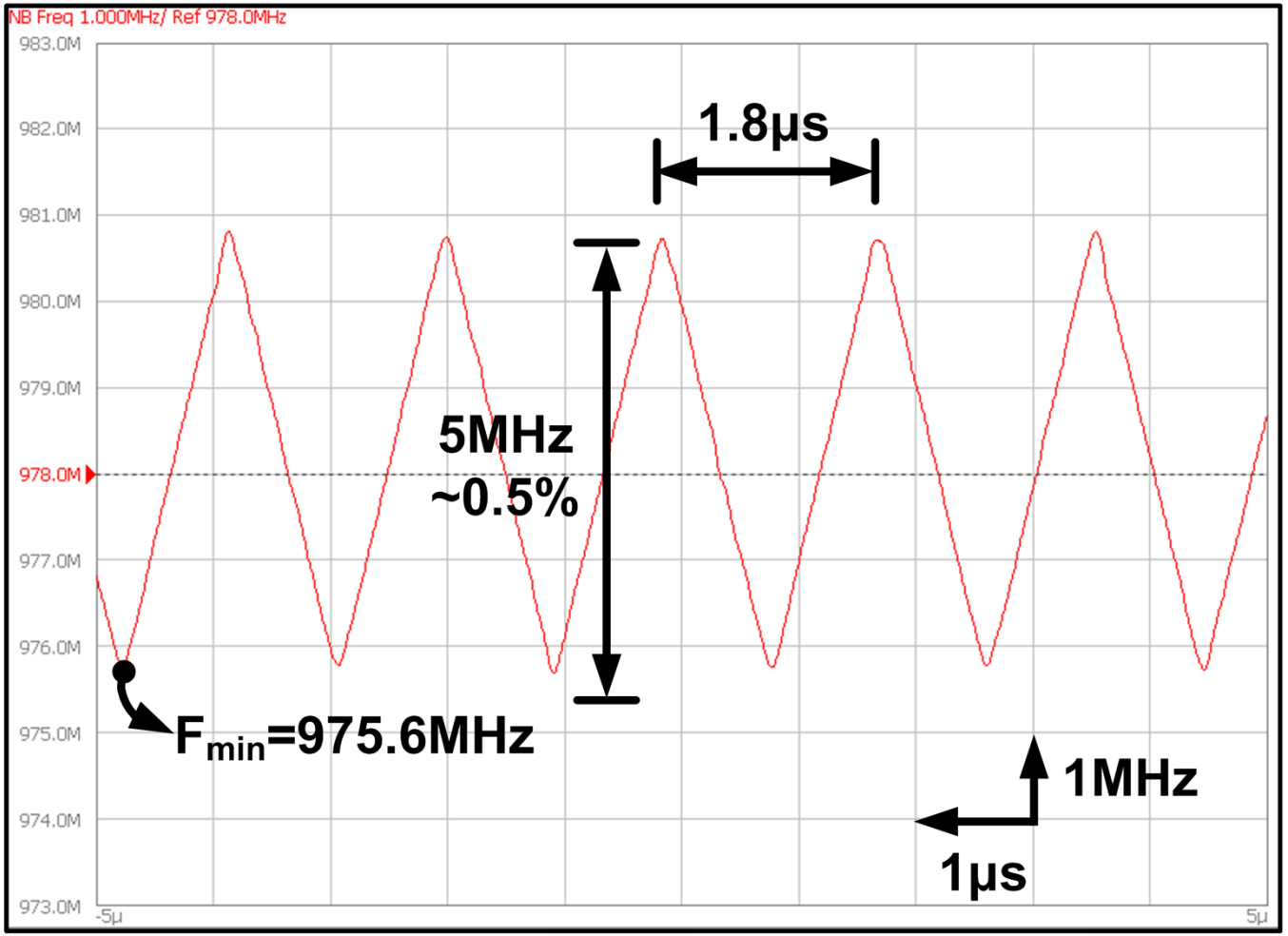
Low Frequency SSC Modulation

- 33kHz triangle modulation, 2% modulation depth



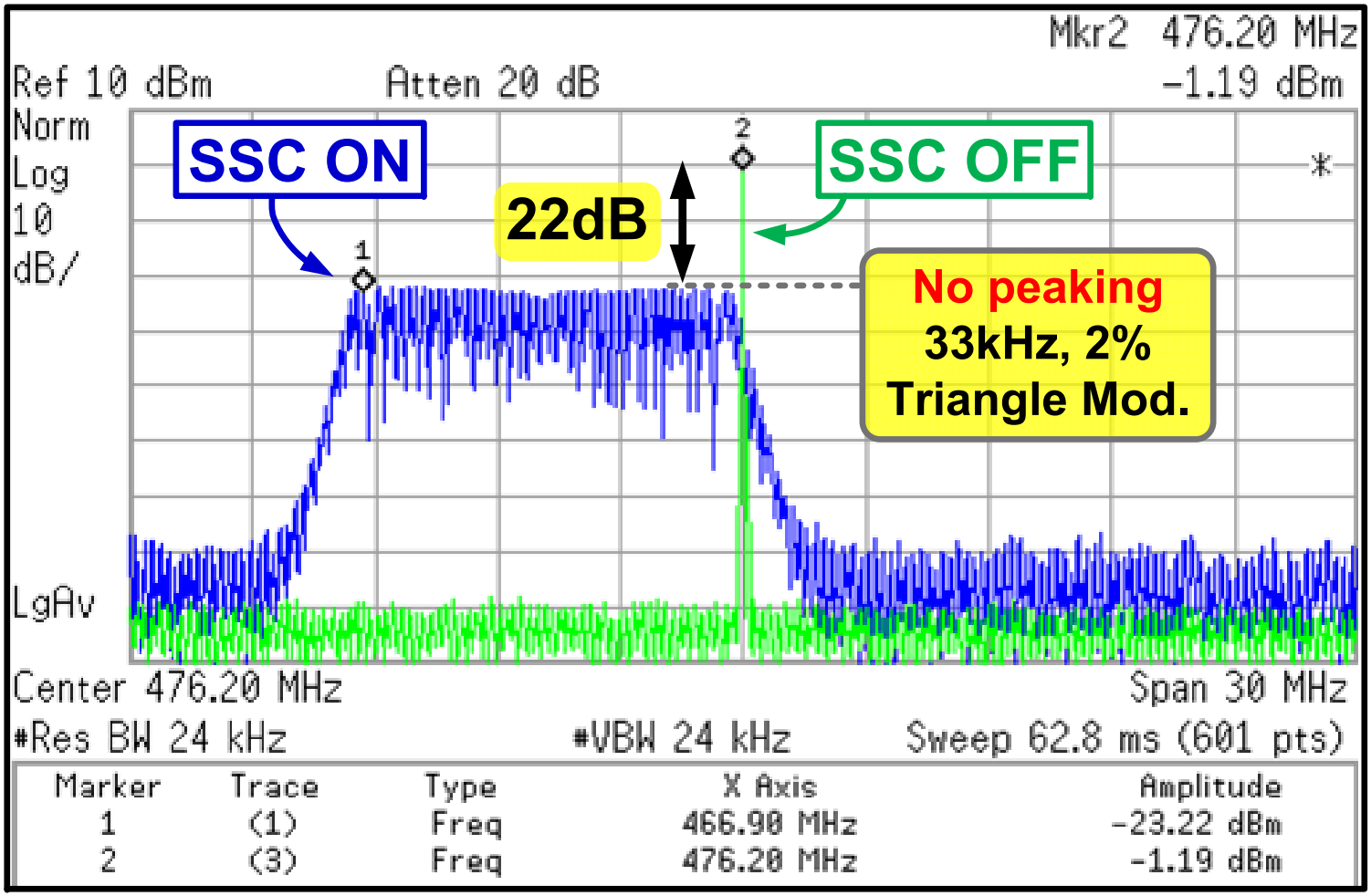
High Frequency SSC Modulation

- 5.5MHz triangle modulation, 0.5% modulation depth



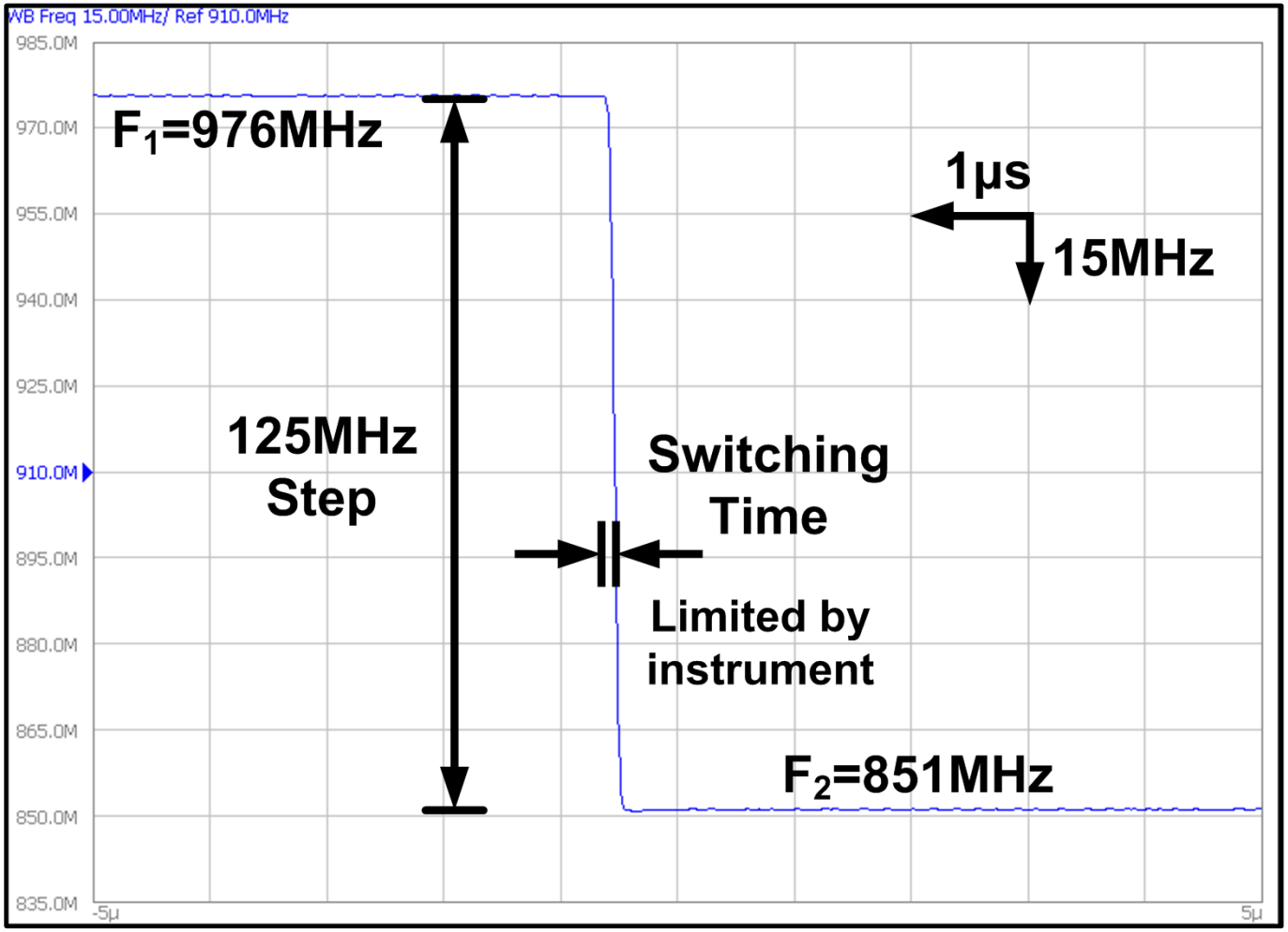
Output Spectrum

- Open-loop modulation produces flat spectrum



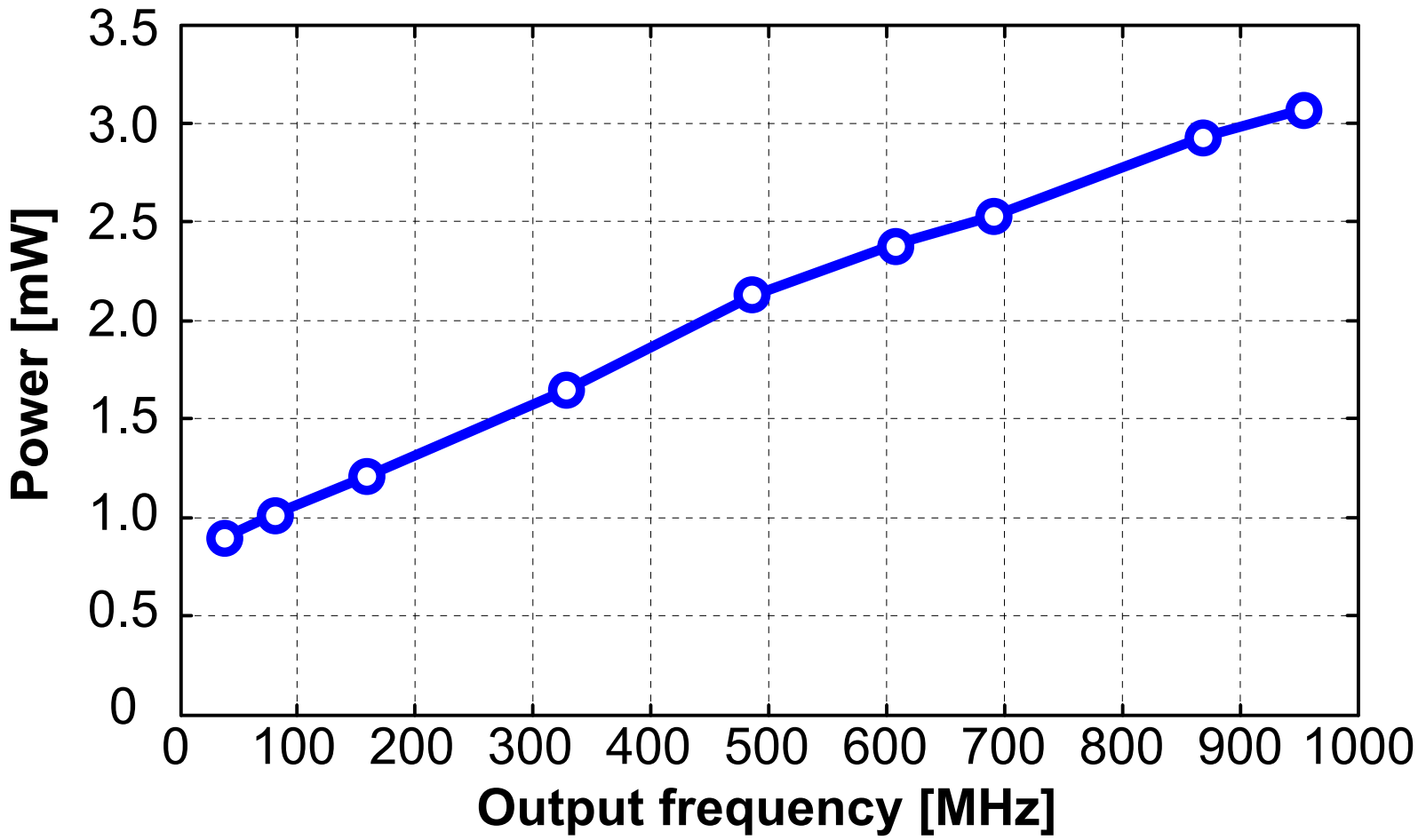
Instantaneous Frequency Switching

- Switching time equals to one cycle (T_{OUT}) ~ 1ns



Power Vs Output Frequency

- Power scales with frequency except MMD



Performance Summary

	This Work	Park ISSCC'12	Li [1] ISSCC'12	De Caro [2] JSSC'10	Grollitsch ISSCC'10	Si labs 5338
Technology	65nm	65nm	22nm	65nm	65nm	N/A
Supply [V]	0.9	1	1	1.2	1.1	1.2
Freq. Range [MHz]	20-1000	580	600-3600	180-1270	375-3025	10-350
RMS Jitter [ps]	3	8.05	10	12.8	5.51	0.7
PP Jitter [ps]	27	N/A	N/A	93	54	13
Instantaneous Switching	Yes	No	No	Yes	No	N/A
SSC Capability	Yes	No	Yes	Yes	Yes	Yes
Power Consumption	3.2mW @1GHz	10.5mW @580MHz	18.4mW @3.6GHz	19.8mW @1.27GHz	3.4mW @751MHz	~13.2mW @350MHz
Power Efficiency [mW/GHz]	3.2	18.1	5.1	15.6	4.1	~37.7
Architecture	Frac-N Divider	Frac-N ILO	Frac-N PLL	DDS	Frac-N PLL	Frac-N Divider
Area [mm^2]	0.017	0.03	0.03	0.044	0.038	N/A

Conclusions

- All-digital generic multi-output clock generator to meet diverse clocking requirements
- Open loop fractional divider architecture
  - ΔΣ quantization cancellation using DCDL
  - DCDL gain background calibration
  - Wide range multi-modulus divider with seamless switching
- Measured results indicate
  - Low peak-to-peak jitter
  - Programmable spread spectrum clocking
  - Instantaneous frequency switching

Acknowledgements

- ***Intel Labs University Research Office***

- ***Semiconductor Research Corporation*** **(SRC) under task 1836.124**

- ***National Science Foundation*** **(NSF) under CAREER EECS-0954969**

- **Berkeley Design Automation provided Analog Fast Spice (AFS) simulator**